HMC833LP6GE

v01.1012

FRACTIONAL-N PLL WITH INTEGRATED VCO 25 - 6000 MHz

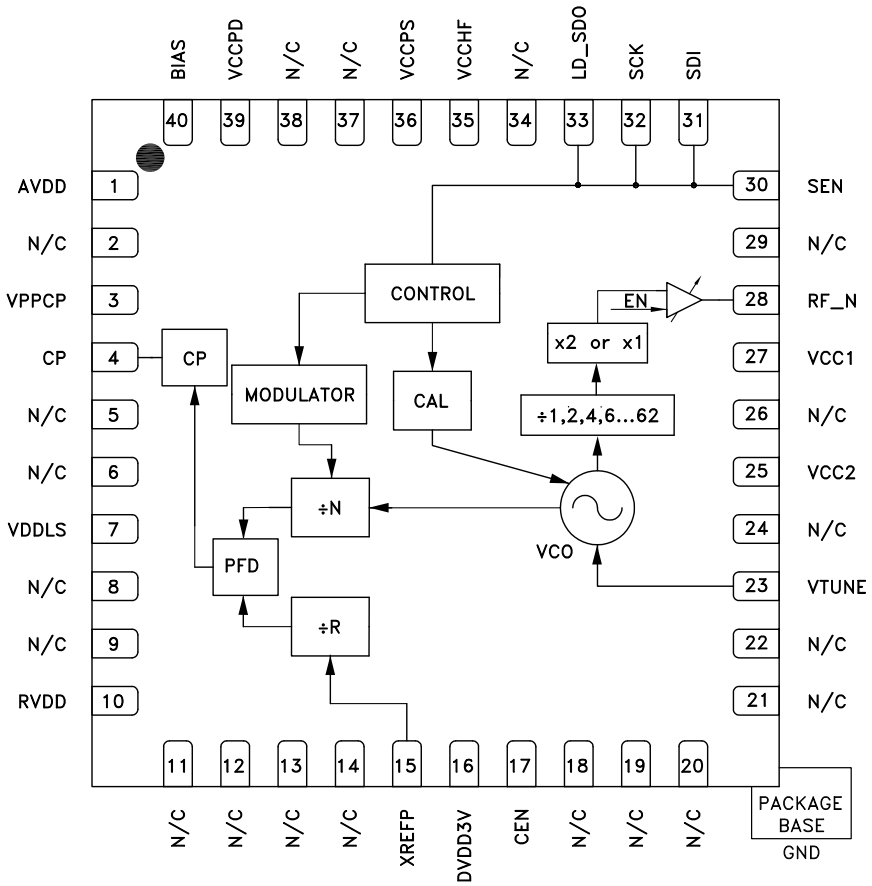
Features

- RF Bandwidth: 25 - 6000 MHz
- Maximum Phase Detector Rate 100 MHz
- Ultra Low Phase Noise -110 dBc/Hz in Band Typ.
- Figure of Merit (FOM) -227 dBc/Hz
- <180 fs RMS Jitter
- 24-bit Step Size, Resolution 3 Hz typ
- Exact Frequency Mode
- Built in Digital Self Test
- 40 Lead 6x6 mm SMT Package: 36 mm^2

Typical Applications

- Cellular Infrastructure
- Microwave Radio
- WiMax, WiFi
- Communications Test Equipment
- CATV Equipment
- DDS Replacement
- Military
- Tunable Reference Source for Spurious-Free Performance

Functional Diagram



FRACTIONAL-N PLL WITH INTEGRATED VCO 25 - 6000 MHz

General Description

The HMC833LP6GE is a low noise, wide band, Fractional-N Phase-Locked-Loop (PLL) that features an integrated Voltage Controlled Oscillator (VCO) with a fundamental frequency of 1500 MHz - 3000 MHz, and an integrated VCO Output Divider (divide by 1/2/4/6.../60/62) and doubler, that together allow the HMC833LP6GE to generate frequencies from 25 MHz to 6000 MHz. The integrated Phase Detector (PD) and delta-sigma modulator, capable of operating at up to 100 MHz, permit wider loop-bandwidths with excellent spectral performance.

The HMC833LP6GE features industry leading phase noise and spurious performance, across all frequencies, that enable it to minimize blocker effects, and improve receiver sensitivity and transmitter spectral purity. The superior noise floor (< -170 dBc/Hz) makes the HMC833LP6GE an ideal source for a variety of applications - such as; LO for RF mixers, a clock source for high-frequency data-converters, or a tunable reference source for ultra-low spurious applications.

Additional features of the HMC833LP6GE include RF output power control from 0 to 9 dB (3 dB steps), output Mute function, and a delta-sigma modulator Exact Frequency Mode which enables users to generate output frequencies with 0 Hz frequency error.

Electrical Specifications

VPPCP, VDDLS, VCC1, VCC2 = 5 V; RVDD, AVDD, DVDD3V, VCCPD, VCCHF, VCCPS = 3.3 V Min and Max Specified across Temp -40 °C to 85 °C

Parameter	Condition	Min.	Typ.	Max.	Units
RF Output Characteristics					
Output Frequency		25		6000	MHz
VCO Frequency at PLL Input		1500		3000	MHz
RF Output Frequency at f_{VCO}		1500		3000	MHz
Output Power					
RF Output Power at $f_{fundamental}$ = 2000 MHz Across All Frequencies see Figure 9	Broadband Matched Internally using Gain control Setting 01 [1]	-3	-2	-1	dBm
Output Power Control Range	[2]	3		9	dB
Output Power Control Step	[2]	1		3	dB
RF Output Power at $f_{doubler}$= 3000 MHz Across All Frequencies see Figure 9	Broadband Matched Internally [1]	-3.5	-2.5	-1.5	dBm
RF Output Power at $f_{doubler}$= 6000 MHz Across All Frequencies see Figure 9	Broadband Matched Internally [1]	-11	-7	-5	dBm
Harmonics for Fundamental Mode					
fo Mode at 2 GHz	2nd / 3rd / 4th		-20/-29/-45		dBc
fo/2 Mode at 2GHz/2 = 1 GHz	2nd / 3rd / 4th		-23/-15/-35		dBc
fo/30 Mode at 3 GHz/30 = 100 MHz	2nd / 3rd / 4th		-25/-10/-33		dBc
fo/62 Mode at 1550 MHz/62 = 25 MHz	2nd / 3rd / 4th		-17/-8/-21		dBc
Harmonics in Doubler Mode					
2fo Mode at 4 GHz	½ / 3rd / 4th/5th		-7/-23/-15/-40		dBc
VCO Output Divider					
VCO RF Divider Range	1,2,4,6,8,...,62	1		62	

[1] Measured single-ended. Additional 3 dB possible with differential outputs.
[2] Output Power Control Gain is compressed in higher frequency range (i.e. > 3 GHz)

Electrical Specifications (Continued)

Parameter	Condition	Min.	Typ.	Max.	Units
PLL RF Divider Characteristics					
19-Bit N-Divider Range (Integer)	Max = 2^{19} - 1	16		524,287	
19-Bit N-Divider Range (Fractional)	Fractional nominal divide ratio varies (-3 / +4) dynamically max	20		524,283	
REF Input Characteristics					
Max Ref Input Frequency				350	MHz
Ref Input Voltage	AC Coupled [3]	1	2	3.3	Vp-p
Ref Input Capacitance				5	pF
14-Bit R-Divider Range		1		16,383	
Phase Detector (PD) [4]					
PD Frequency Fractional Mode B	[5]	DC		100	MHz
PD Frequency Fractional Mode A (and Register 6 [17:16] = 11)		DC		80	MHz
PD Frequency Integer Mode		DC		125	MHz
Charge Pump					
Output Current		0.02		2.54	mA
Charge Pump Gain Step Size			20		µA
PD/Charge Pump SSB Phase Noise	50 MHz Ref, Input Referred				
1 kHz			-143		dBc/Hz
10 kHz	Add 1 dB for Fractional		-150		dBc/Hz
100 kHz	Add 3 dB for Fractional		-153		dBc/Hz
Logic Inputs					
Vsw		40	50	60	% DVDD
Logic Outputs					
VOH Output High Voltage			DVDD		V
VOL Output Low Voltage			0		V
Output Impedance		100		200	Ω
Maximum Load Current				1.5	mA
Power Supply Voltages					
3.3 V Supplies	AVDD, VCCHF, VCCPS, VCCPD, RVDD,DVDD	3.0	3.3	3.5	V
5 V Supplies	VPPCP, VDDLS, VCC1, VCC2	4.8	5	5.2	V
Power Supply Currents					
+5 V Analog Charge Pump	VPPCP, VDDCP		8		mA
+5 V VCO Core and VCO Buffer	fo/1 Mode VCC2		105		mA
	fo/N Mode VCC2		80		mA
+5 V VCO Divider and RF/PLL Buffer	fo/1 Mode VCC1		25		mA
	fo/N Mode VCC1	80		100	mA

[3] Measured with 100 Ω external termination. See "Reference Input Stage" section for more details.
[4] Slew rate of greater or equal to 0.5 ns/V is recommended, see "Reference Input Stage" section for more details. Frequency is guaranteed across process voltage and temperature from -40 °C to 85 °C.
[5] This maximum phase detector frequency can only be achieved if the minimum N value is respected. eg. In the case of fractional B mode, the maximum PFD rate = fvco/20 or 100 MHz, whichever is less.

Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
+3.3 V	AVDD, VCCHF, VCCPS, VCCPD, RVDD, DVDD3V		52		mA
Power Down - Crystal Off	Reg 01h=0, Crystal Not Clocked		10		µA
Power Down - Crystal On, 100 MHz	Reg 01h=0, Crystal Clocked 100 MHz		5		mA
Power on Reset					
Typical Reset Voltage on DVDD			700		mV
Min DVDD Voltage for No Reset		1.5			V
Power on Reset Delay			250		µs
VCO Open Loop Phase Noise at fo @ 2 GHz					
10 kHz Offset			-86		dBc/Hz
100 kHz Offset			-116		dBc/Hz
1 MHz Offset			-141		dBc/Hz
10 MHz Offset			-162		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at fo @ 2 GHz/2 = 1 GHz					
10 kHz Offset			-92		dBc/Hz
100 kHz Offset			-122		dBc/Hz
1 MHz Offset			-147		dBc/Hz
10 MHz Offset			-165		dBc/Hz
100 MHz Offset			-165		dBc/Hz
VCO Open Loop Phase Noise at fo @3 GHz/30 = 100 MHz					
10 kHz Offset			-112		dBc/Hz
100 kHz Offset			-142		dBc/Hz
1 MHz Offset			-165		dBc/Hz
10 MHz Offset			-168		dBc/Hz
100 MHz Offset			-171		dBc/Hz
VCO Open Loop Phase Noise at 2fo @ 4 GHz					
10 kHz Offset			-80		dBc/Hz
100 kHz Offset			-110		dBc/Hz
1 MHz Offset			-135		dBc/Hz
10 MHz Offset			-155		dBc/Hz
100 MHz Offset			-162		dBc/Hz
VCO Open Loop Phase Noise at 2fo @ 6 GHz					
10 kHz Offset			-75		dBc/Hz
100 kHz Offset			-105		dBc/Hz
1 MHz Offset			-131		dBc/Hz
10 MHz Offset			-152		dBc/Hz
100 MHz Offset			-162		dBc/Hz

Electrical Specifications *(Continued)*

Parameter	Condition	Min.	Typ.	Max.	Units
Figure of Merit					
Floor Integer Mode	Normalized to 1 Hz		-230		dBc/Hz
Floor Fractional Mode	Normalized to 1 Hz		-227		dBc/Hz
Flicker (Both Modes)	Normalized to 1 Hz		-268		dBc/Hz
VCO Characteristics					
VCO Tuning Sensitivity at 2800 MHz	Measured at 2.5 V		13.3		MHz/V
VCO Tuning Sensitivity at 2400 MHz	Measured at 2.5 V		13.8		MHz/V
VCO Tuning Sensitivity at 2000 MHz	Measured at 2.5 V		13.6		MHz/V
VCO Tuning Sensitivity at 1600 MHz	Measured at 2.5 V		12.1		MHz/V
VCO Supply Pushing	Measured at 2.5 V		2		MHz/V

Typical Performance Characteristics

Figure 1. Typical Closed Loop Integer Phase Noise ["Loop Filter Configuration Table"]

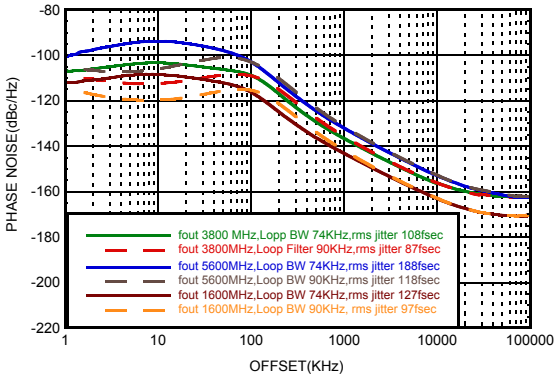


Figure 2. Typical Closed Loop Fractional Phase Noise ["Loop Filter Configuration Table"]

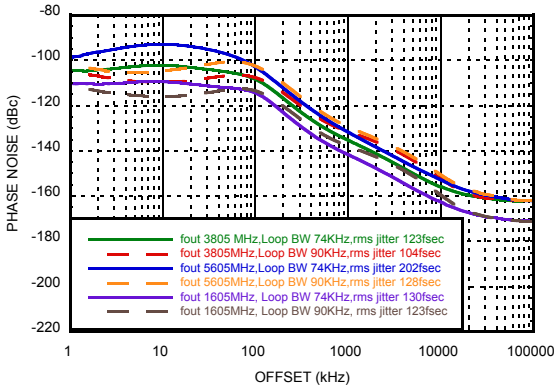


Figure 3. Free Running Phase Noise

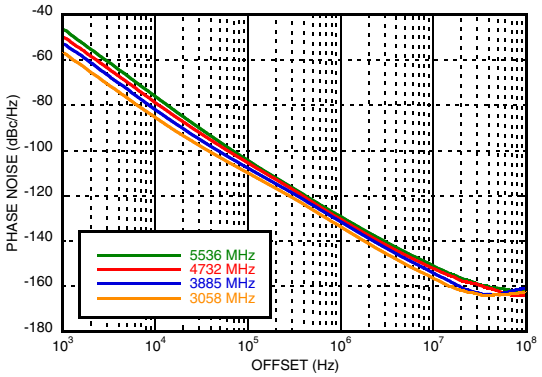


Figure 4. Free Running VCO Phase Noise vs. Temperature

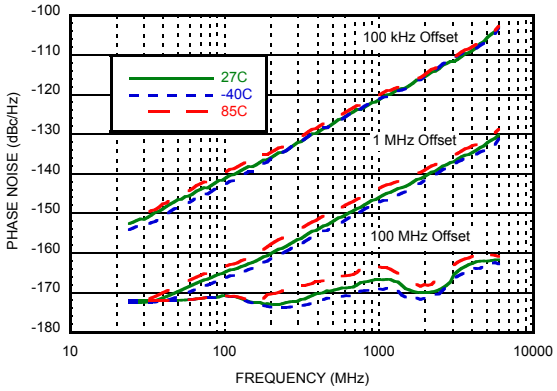


Figure 5. Typical VCO Sensitivity at Fo

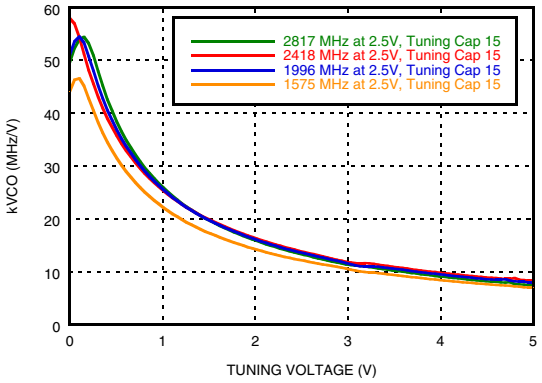


Figure 6. Typical Tuning Voltage After Calibration at Fo

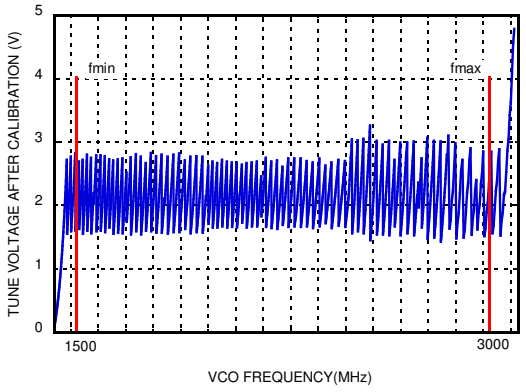


Figure 7. Integrated RMS Jitter[1]

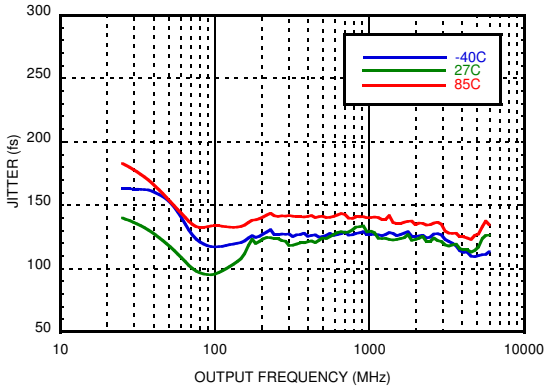


Figure 8. Figure of Merit

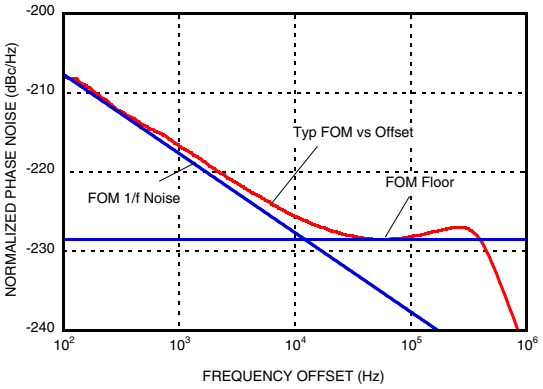


Figure 9. Typical Output Power vs. Temperature, Maximum Gain [2]

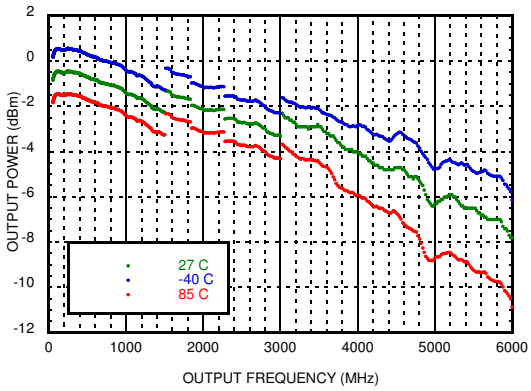


Figure 10. Output Power vs Gain Control Setting

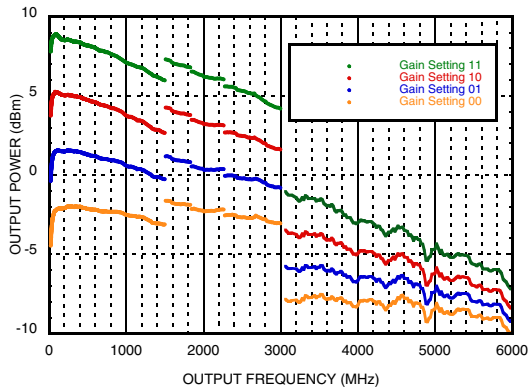


Figure 11. Reference Input Sensitivity, Square Wave, 50 Ω [3]

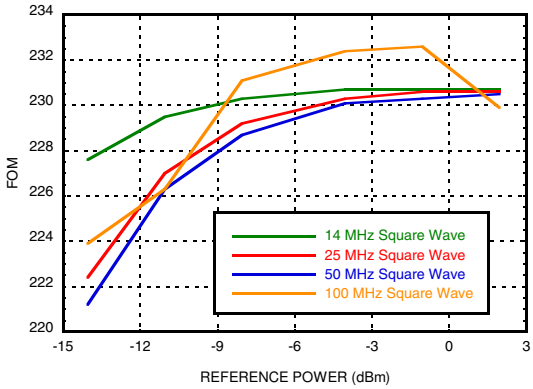
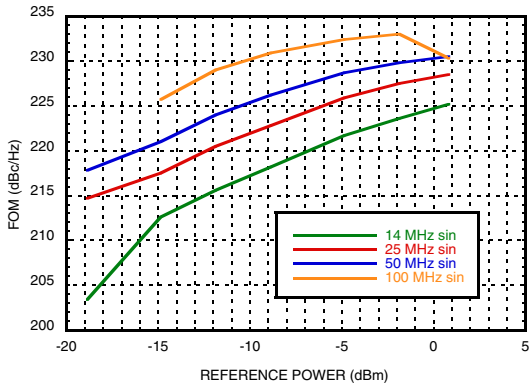


Figure 12. Reference Input Sensitivity Sinusoidal Wave, 50 Ω[3]



[1] RMS Jitter data is measured in fractional mode with 100 kHz Loop bandwidth using 50 MHz reference frequency from 1 kHz to 20 MHz integration bandwidth.

[2] The output power from Frequency 25MHz to 3000MHz is using fundamental Configuration with Gain Setting 01, output power from Frequency 3000MHz to 6000MHz is using doubler Configuration with Gain Setting 11

[3] Measured from a 50 Ω source with a 100 Ω external resistor termination. See "Reference Input Stage" section for more details. Full FOM performance up to maximum 3.3 Vpp input voltage.

Figure 13. Integer Boundary Spur at 5900.8 MHz[4]

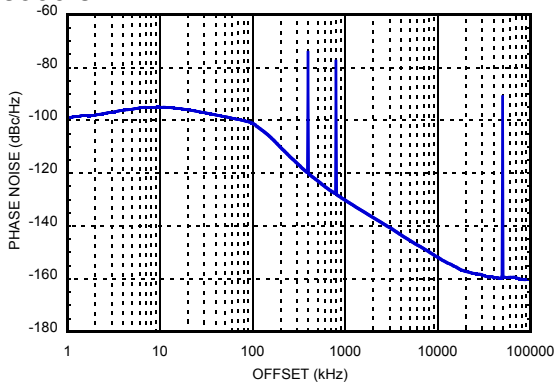


Figure 14. Integer Boundary Spur at 3800.4 MHz [5]

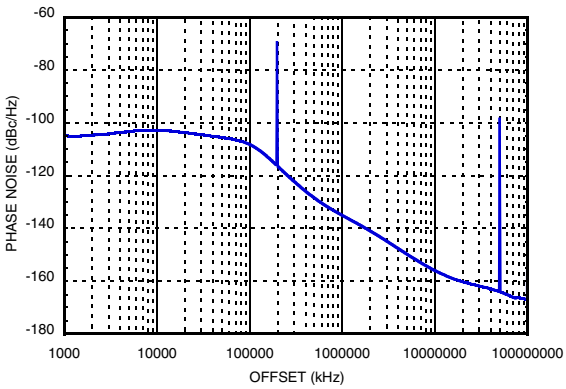


Figure 15. Fractional-N Exact Frequency Mode ON Performance at 2113.5 MHz[6]

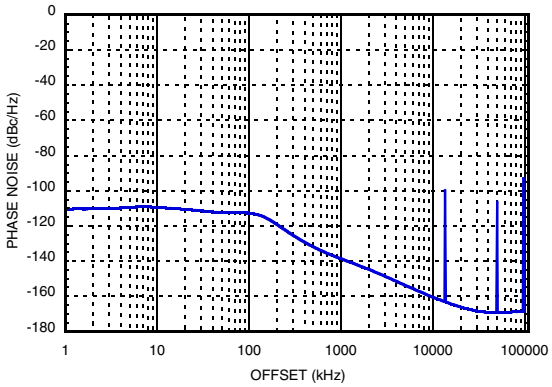


Figure 16. Fractional-N Exact Frequency Mode ON Performance at 2591 MHz[7]

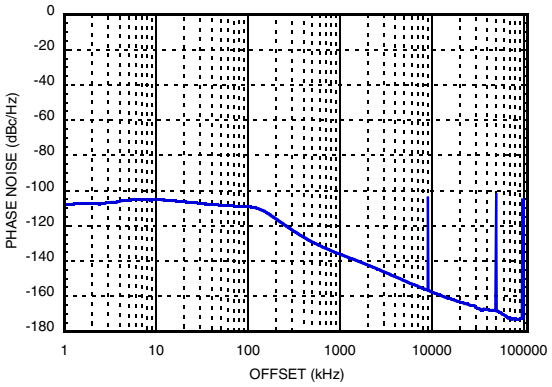


Figure 17. Fractional-N Exact Frequency Mode OFF Performance at 2591 MHz[8]

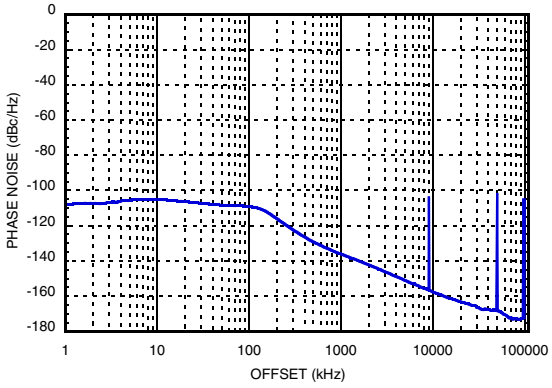
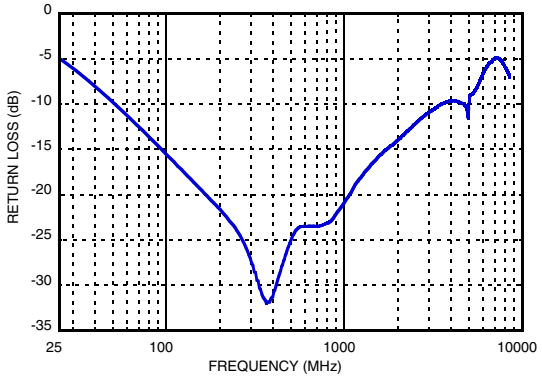


Figure 18. RF Output Return Loss



[4] Fractional Mode B, 50 MHz PD frequency, 74 kHz Loop Filter BW
[5] Fractional Mode B, 50 MHz PD frequency, 74 kHz Loop Filter BW Integer Boundary at 3800 MHz
[6] Exact Frequency Mode, REF in = 100 MHz, PD = 50 MHz, Output Divider 1 Selected, Loop Filter bandwidth = 100 kHz, Channel Spacing = 100 kHz
[7] Exact Frequency Mode, Channel Spacing = 100 kHz, Fractional Mode B RF out = 2591 MHz, REF in = 100 MHz, PD frequency = 50 MHz, Output Divider 1 selected, Loop Filter bandwidth = 120 kHz,
[8] Fractional Mode B RF out = 2591 MHz, REF in = 100 MHz, PD frequency = 50 MHz, Output Divider 1 selected, Loop Filter bandwidth = 120 kHz.

Figure 19. Worst Spur, Fixed 50 MHz Reference, Output Freq. = 2000.1 MHz[9]

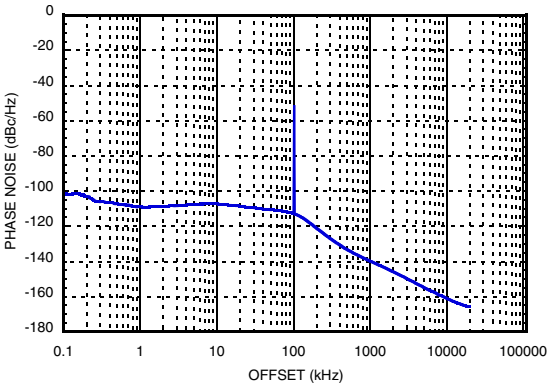


Figure 20. Worst Spur, Tunable Reference, Output Frequency = 2000.1 MHz [10]

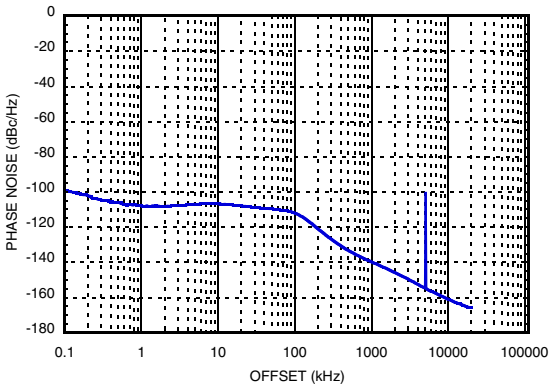


Figure 21. Low Frequency Performance [12]

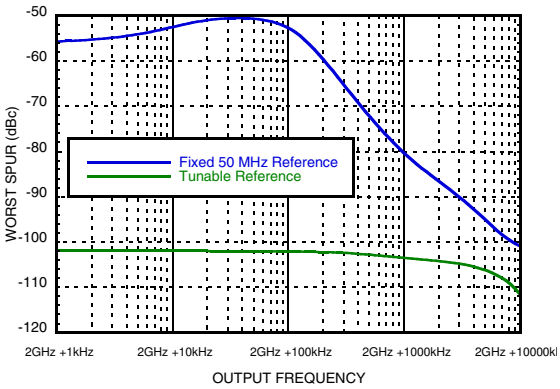
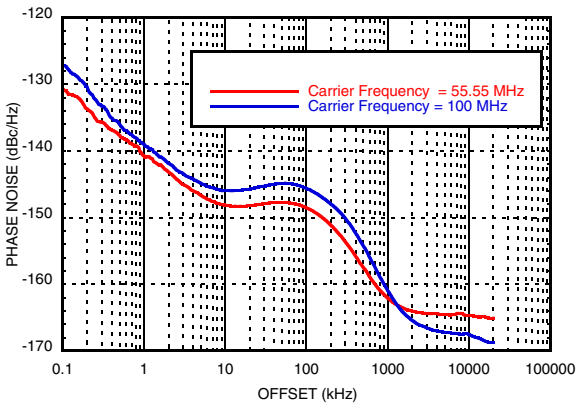


Figure 22. Low Frequency Performance [12]



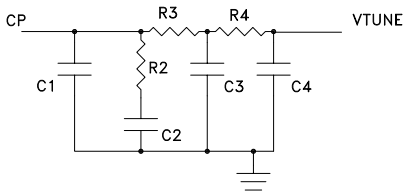
[9] Standard HMC830LP6GE integer boundary spur plot with fix PFD at 50 MHz

[10] Capability of HMC830LP6GE to generate low frequencies (as low as 25 MHz), enables the HMC830LP6GE to be used as a tunable reference source into the HMC833LP6GE, which maximizes spur performance of the HMC833LP6GE. Please see "HMC833LP6GE Application Information" for more information.

[11] The graph is generated by observing, and plotting, the magnitude of only the worst spur (largest magnitude), at any offset, at each output frequency, while using a fixed 50 MHz reference and a tunable reference tuned to 47.5 MHz. See "HMC833LP6GE Application Information" for more details.

[12] Phase noise performance of the HMC833LP6GE when used as a tunable reference source. HMC833LP6GE is operating at 6 GHz/30, 6 GHz/54 for the 100 MHz, 55.55 MHz curves respectively.

Loop Filter Configuration Table

Loop Filter BW (kHz)	C1 (pF)	C2 (nF)	C3 (pF)	C4 (pF)	R2 (kΩ)	R3 (kΩ)	R4 (kΩ)	Loop Filter Design
74	150	27	220	220	0.82	1	1	
90	270	3.9	56	56	1.2	1	1	
214	56	1.8	NA	NA	2.2	0	0	

Pin Descriptions

Pin Number	Function	Description
1	AVDD	DC Power Supply for analog circuitry.
2, 5, 6, 8, 9, 11 - 14, 18 - 22, 24, 26, 29, 34, 37, 38	N/C	The pins are not connected internally; however, all data shown herein was measured with these pins connected to RF/DC ground externally.
3	VPPCP	Power Supply for charge pump analog section
4	CP	Charge Pump Output
7	VDDLS	Power Supply for the charge pump digital section
10	RVDD	Reference Supply
15	XREFP	Reference Oscillator Input
16	DVDD3V	DC Power Supply for Digital (CMOS) Circuitry
17	CEN	Chip Enable. Connect to logic high for normal operation.
23	VTUNE	VCO Varactor. Tuning Port Input.
25	VCC2	VCO Analog Supply 2
27	VCC1	VCO Analog Supply 1
28	RF_N	RF Output
30	SEN	PLL Serial Port Enable (CMOS) Logic Input
31	SDI	PLL Serial Port Data (CMOS) Logic Input
32	SCK	PLL Serial Port Clock (CMOS) Logic Input
33	LD_SDO	Lock Detect, or Serial Data, or General Purpose (CMOS) Logic Output (GPO)
35	VCCHF	DC Power Supply for Analog Circuitry
36	VCCPS	DC Power Supply for Analog Prescaler
39	VCCPD	DC Power Supply for Phase Detector
40	BIAS	External bypass decoupling for precision bias circuits. Note: 1.920V ±20mV reference voltage (BIAS) is generated internally and cannot drive an external load. Must be measured with 10GΩ meter such as Agilent 34410A, normal 10MΩ DVM will read erroneously.

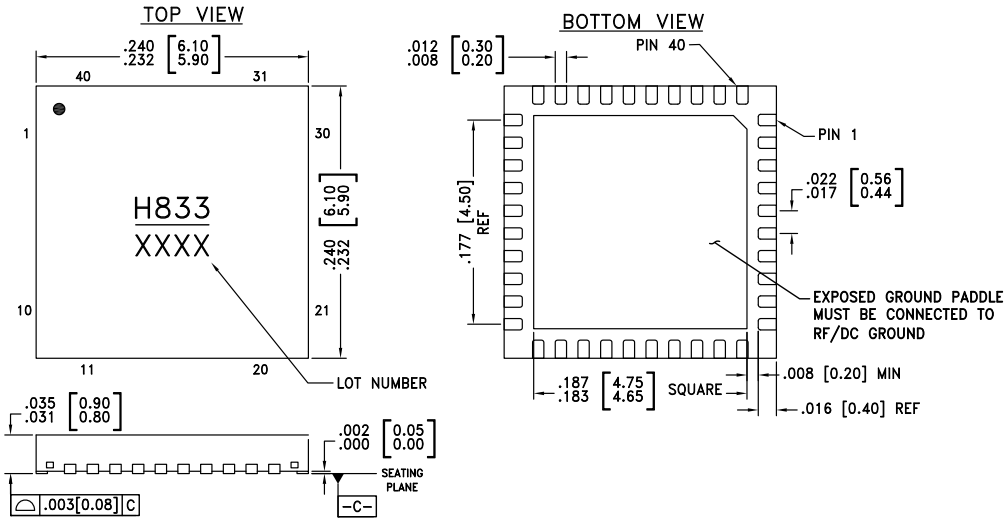
FRACTIONAL-N PLL WITH INTEGRATED VCO 25 - 6000 MHz

Absolute Maximum Ratings

AVDD, RVDD, DVDD3V, VCCPD, VCCHF, VCCPS	-0.3V to +3.6V
VPPCP, VDDLS, VCC1,VCC2	-0.3V to +5.5V
Operating Temperature	-40°C to +85°C
Storage Temperature	-65°C to 150°C
Maximum Junction Temperature	125 °C
Thermal Resistance (R_{TH}) (junction to ground paddle)	20 °C/W
Reflow Soldering	
Peak Temperature	260°C
Time at Peak Temperature	40 sec
ESD Sensitivity (HBM)	Class 1B

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Outline Drawing



NOTES:

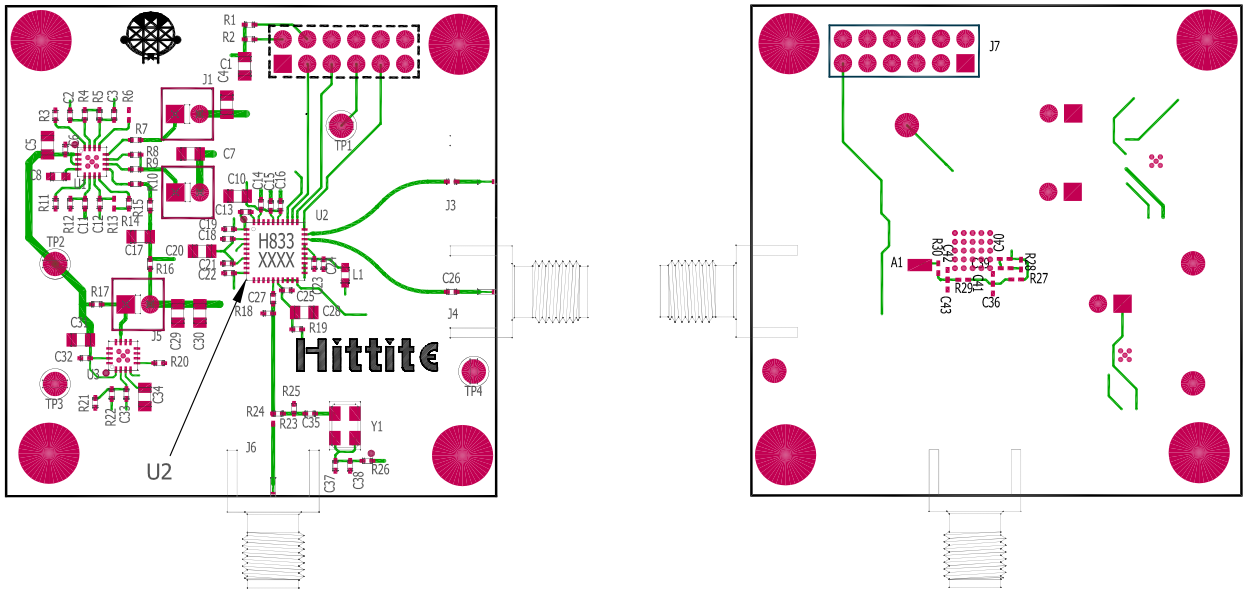
1. PACKAGE BODY MATERIAL: LOW STRESS INJECTION MOLDED PLASTIC SILICA AND SILICON IMPREGNATED.
2. LEAD AND GROUND PADDLE MATERIAL: COPPER ALLOY.
3. LEAD AND GROUND PADDLE PLATING: 100% MATTE TIN.
4. DIMENSIONS ARE IN INCHES [MILLIMETERS].
5. LEAD SPACING TOLERANCE IS NON-CUMULATIVE.
6. PAD BURR LENGTH SHALL BE 0.15mm MAX. PAD BURR HEIGHT SHALL BE 0.25mm MAX.
7. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
8. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
9. REFER TO HITTITE APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC833LP6GE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1	H833 XXXX

[1] 4-Digit lot number XXXX

Evaluation PCB



The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

Evaluation PCB Schematic

To view this Evaluation PCB Schematic please visit www.hittite.com and choose HMC833LP6GE from the "Search by Part Number" pull down menu to view the product splash page.

Evaluation Order Information

Item	Contents	Part Number
Evaluation Kit	HMC833LP6GE Evaluation PCB USB Interface Board 6' USB A Male to USB B Female Cable CD ROM (Contains User Manual, Evaluation PCB Schematic, Evaluation Software, Hittite PLL Design Software)	EKIT01-HMC833LP6GE

HMC833LP6GE Application Information

Large bandwidth (25 MHz to 6000 MHz), industry leading phase noise and spurious performance, excellent noise floor (<-170 dBc/Hz), coupled with a high level of integration make the HMC833LP6GE ideal for a variety of applications; as an RF or IF stage LO, a clock source for high-frequency data-converters, or a tunable reference source for extremely low spurious applications (< -100 dBc/Hz spurs).

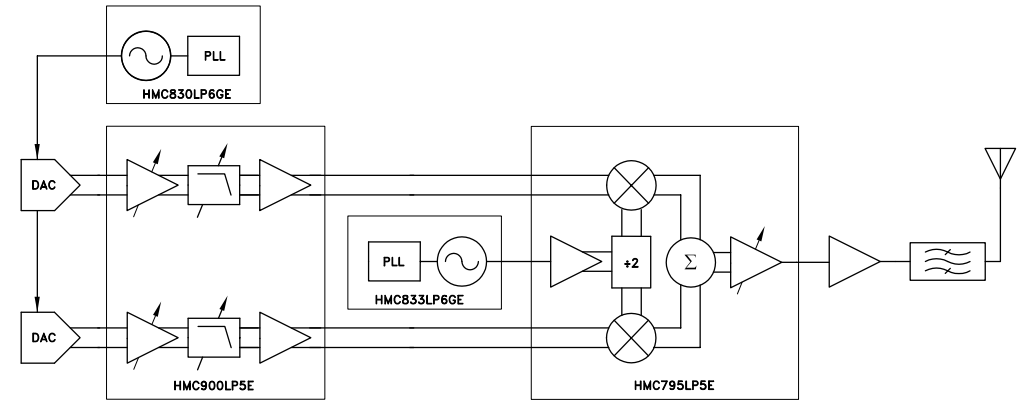


Figure 27. HMC833LP6GE in a typical transmit chain

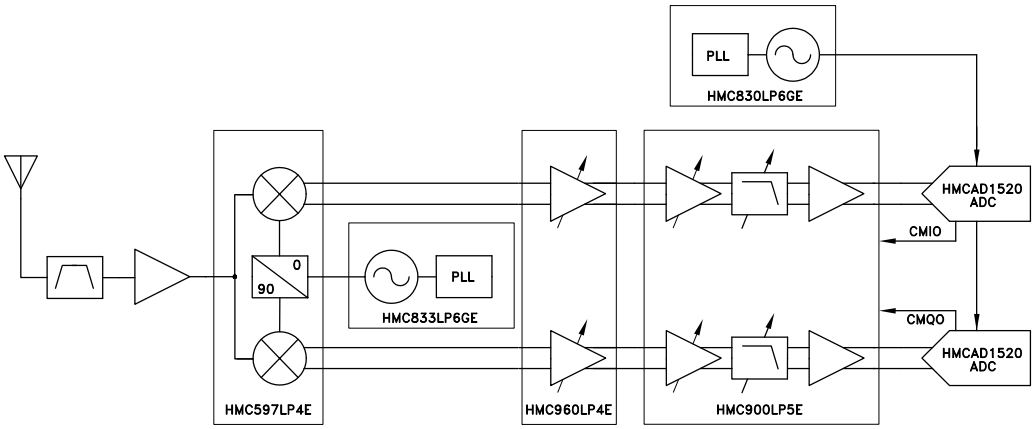


Figure 28. HMC833LP6GE in a typical receive chain

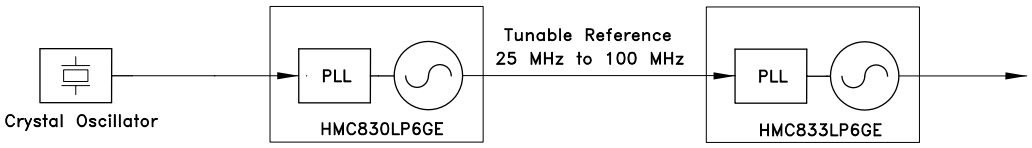


Figure 29. HMC830LP6GE used as a tunable reference for HMC833LP6GE

Using the HMC833LP6GE with a tunable reference as shown in Figure 25, it is possible to drastically improve spurious emissions performance across all frequencies. Example shown in Figure 20 graph shows that it is possible to have spurious emissions < -100 dBc/Hz across all frequencies. For more information about spurious emissions, how they are related to the reference frequency, and how to tune the reference frequency for optimal spurious performance please see the "Fractional Operation and Spurious" section of this data sheet. Note that at very low output frequencies < 100 MHz, harmonics increase due to small internal AC coupling. Applications which are sensitive to harmonics may require external low pass filtering.

Output gain setting for Optimal Power Flatness

The output of the HMC833LP6GE is matched to 50 Ω across all output frequencies from 25 MHz to 6000 MHz. As a result of the wideband 50 Ω match, the output power of the HMC833LP6GE decreases with increasing output frequency, as shown in Figure 9. If required, it is possible to adjust the output stage gain setting of the HMC833LP6GE (VCO_Reg 02h[7:6]) at various operating frequencies in order to achieve a more constant output power level across the frequency operating range of the HMC833LP6GE. An example is shown in Figure 26.

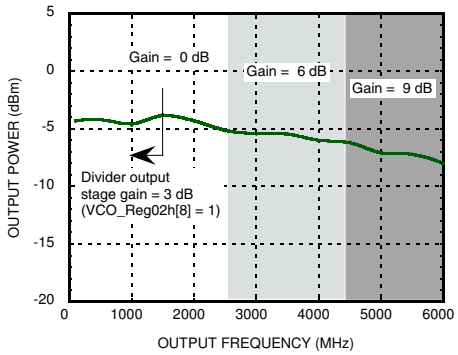


Figure 30. Reducing the output power variation of HMC833LP6GE across frequency by adjusting output stage gain control.

If a higher output power than that shown in Figure 26 is required, it is possible to follow the HMC833LP6GE output stage with a simple amplifier such as HMC311SC70E in order to achieve a constant and high output power level across the entire operating range of the HMC833LP6GE.

1.0 Theory of Operation

HMC833LP6GE is targeted for ultra low phase noise applications and has been designed with very low noise reference path, phase detector and charge pump.

The HMC833LP6GE consists of the following functional blocks:

1. Reference Path Input Buffers and 'R' Divider
2. VCO Path Input Buffer and Multi-Modulus 'N' Divider
3. ΔΣ Fractional Modulator
4. Phase Detector
5. Charge Pump
6. Serial Port with Read Write Capability
7. General Purpose Output (GPO) Port
8. Power On Reset Circuit
9. VCO Subsystem
10. Built-In Self Test Features

1.1 VCO Subsystem

The HMC833LP6GE contains a VCO subsystem that can be configured to operate in:

- Fundamental frequency (fo) mode (1500 MHz to 3000 MHz).
- Divide by N (fo/N), where N = 1,2,4,6,8...58,60,62 mode (25 MHz to 1500 MHz).
- Doubler (2fo) mode (3000 MHz to 6000 MHz).

All modes are VCO register programmable as shown in Figure 27. One loop filter design can be used for the entire frequency of operation of the HMC833LP6GE.

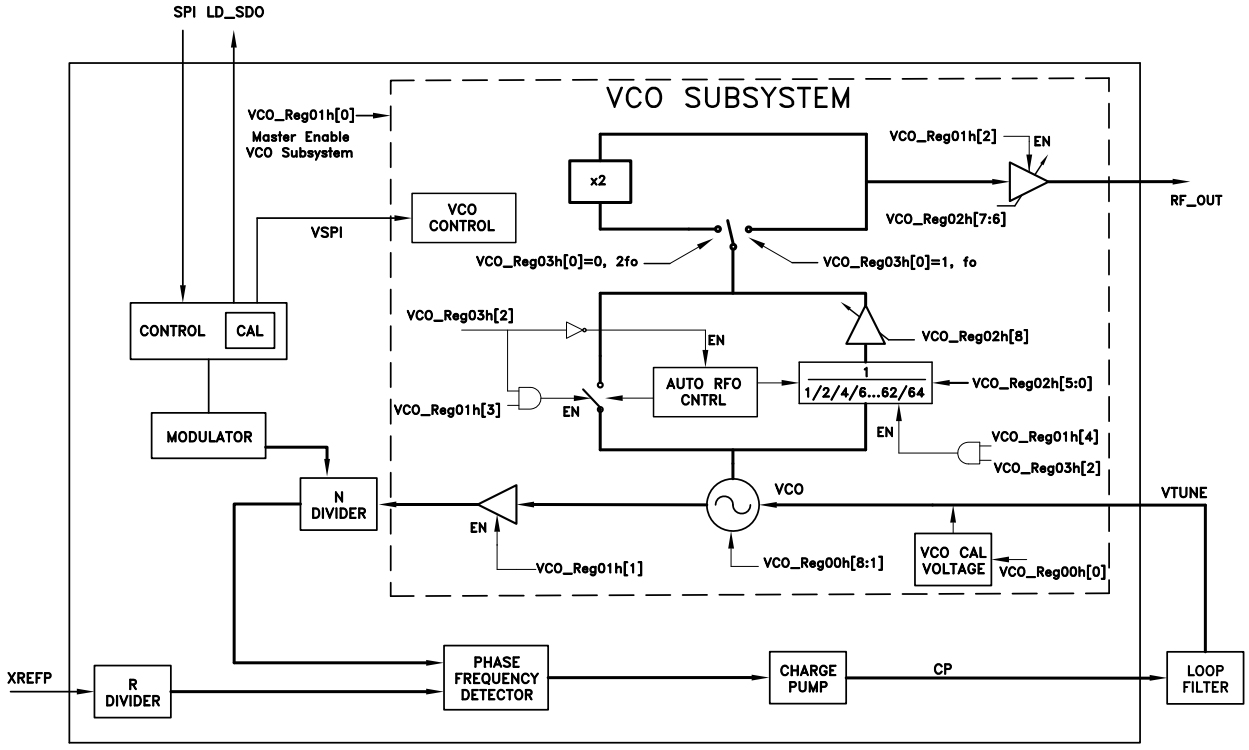


Figure 31. PLL and VCO Subsystems

1.2 VCO Calibration

1.2.1 VCO Auto-Calibration (AutoCal)

HMC833LP6GE uses a step tuned type VCO. A simplified step tuned VCO is shown in Figure 28. A step tuned VCO is a VCO with a digitally selectable capacitor bank allowing the nominal center frequency of the VCO to be adjusted or 'stepped' by switching in/out VCO tank capacitors. A more detailed view of a typical VCO subsystem configuration is shown in Figure 29. A step tuned VCO allows the user to center the VCO on the required output frequency while keeping the varactor tuning voltage optimized near the mid-voltage tuning point of the HMC833LP6GE's charge pump. This enables the PLL charge pump to tune the VCO over the full range of operation with both a low tuning voltage and a low tuning sensitivity (kvco).

The VCO switches are normally controlled automatically by the HMC833LP6GE using the Auto-Calibration feature. The Auto-Calibration feature is implemented in the internal state machine. It manages the selection of the VCO sub-band (capacitor selection) when a new frequency is programmed. The VCO switches may also be controlled directly via register Reg 05h for testing or for other special purpose operation. Other control bits specific to the VCO are also sent via Reg 05h.

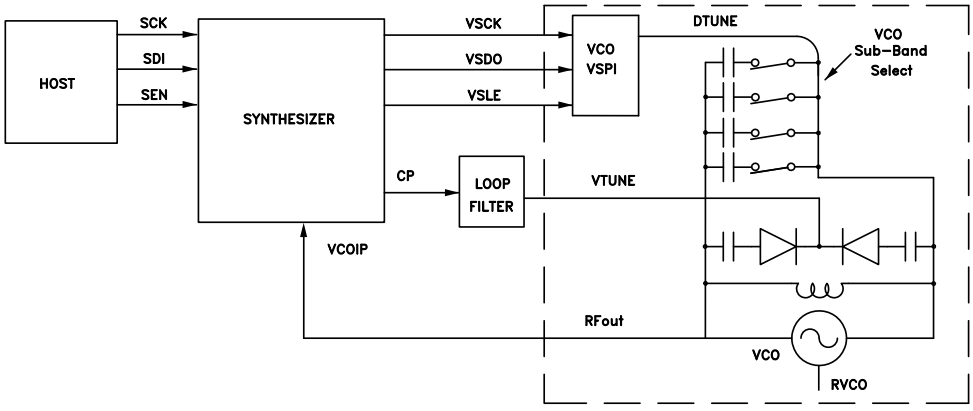


Figure 32. Simplified Step Tuned VCO

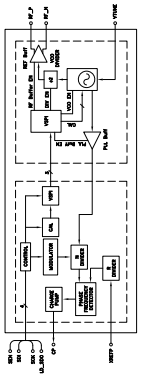


Figure 33. HMC833LP6GE PLL and VCO Subsystems

To use a step tuned VCO in a closed loop, the VCO must be calibrated such that the HMC833LP6GE knows which switch position on the VCO is optimum for the desired output frequency. The HMC833LP6GE supports Auto-Calibration (AutoCal) of the step tuned VCO. The AutoCal fixes the VCO tuning voltage at the optimum mid-point of the charge pump output, then measures the free running VCO frequency while searching for the setting which results in the free running output frequency that is closest to the

desired phase locked frequency. This procedure results in a phase locked oscillator that locks over a very narrow voltage range on the varactor. A typical tuning curve for a step tuned VCO is shown in Figure 30. Note how the tuning voltage stays in a narrow range over a wide range of output frequencies.

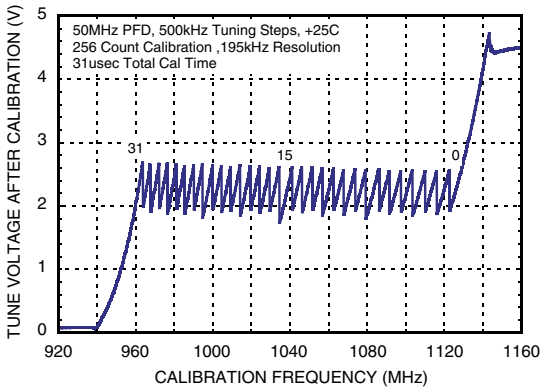


Figure 34. A Typical 5-Bit 32 Switch VCO Tuning Voltage After Calibration

The calibration is normally run automatically once for every change of frequency. This ensures optimum selection of VCO switch settings vs. time and temperature. The user does not normally have to be concerned about which switch setting is used for a given frequency as this is handled by the AutoCal routine. The accuracy required in the calibration affects the amount of time required to tune the VCO. The calibration routine searches for the best step setting that locks the VCO at the current programmed frequency, and ensures that the VCO will stay locked and perform well over it's full temperature range without additional calibration, regardless of the temperature that the VCO was calibrated at.

Auto-Calibration can also be disabled allowing manual VCO tuning. Refer to section 1.2.2 for a description of manual tuning

1.2.1.1 AutoCal Use of Reg05h

AutoCal transfers switch control data to the VCO subsystem via Reg 05h. The address of the VCO subsystem in Reg 05h is not altered by the AutoCal routine. The address and ID of the VCO subsystem in Reg 05h must be set to the correct value before AutoCal is executed. For more information see section 1.19.

1.2.1.2 Auto-reLock on Lock Detect Failure

It is possible by setting Reg 07h*[13]* to have the VCO subsystem automatically re-run the calibration routine and re-lock itself if Lock Detect indicates an unlocked condition for any reason. With this option the system will attempt to re-Lock only once. Auto-reLock is recommended.

1.2.2 Manual VCO Calibration for Fast Frequency Hopping

If it is desirable to switch frequencies very quickly it is possible to eliminate the AutoCal time by calibrating the VCO in advance and storing the switch number vs frequency information in the host. This can be done by initially locking the PLL with Integrated VCO on each desired frequency using AutoCal, then reading, and storing the VCO switch settings selected. The VCO switch settings are available in Reg 10h[7:0] after every AutoCal operation. The host must then program the VCO switch settings directly when changing frequencies. Manual writes to the VCO switches are executed immediately as are writes to the integer and fractional registers when AutoCal is disabled. Hence frequency changes with manual control and AutoCal disabled, requires a minimum of two serial port transfers to the PLL, once to set the VCO switches, and once to set the PLL frequency.

If AutoCal is disabled Reg 0Ah*[11]=1*, the VCO will update its registers with the value written via Reg 05h immediately. The VCO internal transfer requires 16 VSCK clock cycles after the completion of a write to Reg 05h. VSCK and the AutoCal controller clock are equal to the input reference divided by 0, 4,16 or 32 as controlled by Reg 0Ah*[14:13]*.

1.2.2.1 Registers required for Frequency Changes in Fractional Mode

A large change of frequency, in fractional mode (Reg 06h*[11]=1*), may require Main Serial Port writes to:

1. the integer register intg, Reg 03h *(only required if the integer part changes)*
2. the VCO SPI register, Reg 05h
   - required for manual control of VCO if Reg 0Ah*[11]=1 (AutoCal disabled)*
   - required to change the RF Divider value if needed (VCO_Reg 02h)
   - required to turn on/off the doubler mode if needed (VCO_Reg 03h[0])
3. the fractional register, Reg 04h. The fractional register write triggers AutoCal if Reg 0Ah*[11]=0*, and is loaded into the modulator automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah*[11]=1*, the fractional frequency change is loaded into the modulator immediately when the register is written with no adjustment to the VCO.

Small steps in frequency in fractional mode, with AutoCal enabled (Reg 0Ah*[11]=0*), usually only require a single write to the fractional register. Worst case, 5 Main Serial Port transfers to the HMC833LP6GE could be required to change frequencies in fractional mode. If the frequency step is small and the integer part of the frequency does not change, then the integer register is not changed. In all cases, in fractional mode, it is necessary to write to the fractional register Reg 04h for frequency changes.

1.2.2.2 Registers Required for Frequency Changes in Integer Mode

A change of frequency, in integer mode *(*Reg 06h*[11]=0)*, requires Main Serial Port writes to:

1. VCO SPI register, Reg 05h
   - required for manual control of VCO if Reg 0Ah*[11]=1 (AutoCal disabled)*
   - required to change the RF Divider value if needed (VCO_Reg 02h)
   - required to turn on/off the doubler mode if needed (VCO_Reg 03h[0])
2. the integer register Reg 03h.
   - In integer mode, an integer register write triggers AutoCal if Reg 0Ah*[11]=0*, and is loaded into the prescaler automatically after AutoCal runs. If AutoCal is disabled, Reg 0Ah*[11]=1*, the integer frequency change is loaded into the prescaler immediately when written with no adjustment to the VCO. Normally changes to the integer register cause large steps in the VCO frequency, hence the VCO switch settings must be adjusted. AutoCal enabled is the recommended method for integer mode frequency changes. If AutoCal is disabled (Reg 0Ah*[11]=1*), a priori knowledge of the correct VCO switch setting and the corresponding adjustment to the VCO is required before executing the integer frequency change.

1.2.3 VCO AutoCal on Frequency Change

Assuming Reg 0Ah*[11]=0*, the VCO calibration starts automatically whenever a frequency change is requested. If it is desired to rerun the AutoCal routine for any reason, at the same frequency, simply rewrite the frequency change with the same value and the AutoCal routine will execute again without changing final frequency.

1.2.4 VCO AutoCal Time & Accuracy

The VCO frequency is counted for T_{mmt}, the period of a single AutoCal measurement cycle.

$$T_{mmt} = T_{xtal} \cdot R \cdot 2^n \quad \text{(EQ 1)}$$

n is set by Reg 0Ah*[2:0]* and results in measurement periods which are multiples of the PD period, $T_{xtal}R$.

R is the reference path division ratio currently in use, Reg 02h

T_{xtal} is the period of the external reference (crystal) oscillator.

The VCO AutoCal counter will, on average, expect to register N counts, rounded down (floor) to the nearest integer, every PD cycle.

N is the ratio of the target VCO frequency, f_{vco}, to the frequency of the PD, f_{pd}, where N can be any rational number supported by the N divider.

N is set by the integer (N_{int} = Reg 03h) and fractional (N_{frac} = Reg 04h) register contents

$$N = N_{int} + N_{frac} / 2^{24} \quad \text{(EQ 2)}$$

The AutoCal state machine and the data transfers to the internal VCO subsystem SPI (VSPI) run at the rate of the FSM clock, T_{FSM}, where the FSM clock frequency cannot be greater than 50 MHz.

$$T_{FSM} = T_{xtal} \cdot 2^m \quad \text{(EQ 3)}$$

m is 0, 2, 4 or 5 as determined by Reg 0Ah*[14:13]*

The expected number of VCO counts, V, is given by

$$V = floor\ (N \cdot 2^n) \quad \text{(EQ 4)}$$

The nominal VCO frequency measured, f_{vcom}, is given by

$$f_{vcom} = V \cdot f_{xtal} / (2^n \cdot R) \quad \text{(EQ 5)}$$

where the worst case measurement error, f_{err} , is:

$$f_{err} \approx \pm f_{pd} / 2^{n+1} \quad \text{(EQ 6)}$$

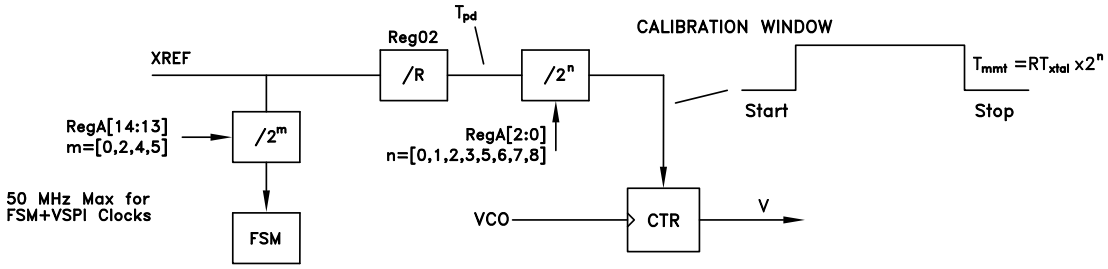


Figure 35. VCO Calibration

A 5-bit step tuned VCO, for example, nominally requires 5 measurements for calibration, worst case 6 measurements, and hence 7 VSPI data transfers of 20 clock cycles each. The measurement has a programmable number of wait states, k, of 100 FSM cycles defined by Reg 0Ah[7:6] = k. Hence total calibration time, worst case, is given by:

$$T_{cal} = k100T_{FSM} + 6T_{PD}\ 2^n + 7 \cdot 20T_{FSM} \quad \text{(EQ 7)}$$

or equivalently

$$T_{cal} = T_{xtal}\,(6R \cdot 2^{n} + (140+100k) \cdot 2^{m}) \quad \text{(EQ 8)}$$

where k = Reg 0Ah*[7:6] decimal*

For guaranteed hold of lock, across temperature extremes, the resolution should be better than 1/8th the frequency step caused by a VCO sub-band switch change. Better resolution settings will show no improvement.

1.2.4.1 VCO AutoCal Example

The VCO subsystem must satisfy the maximum f_{pd} limited by the two following conditions:

a. N ≥ 16 (f_{int}), N ≥ 20.0 (f_{frac}), where N = f_{VCO}/ f_{pd}

b. f_{pd} ≤ 100 MHz

Suppose the VCO subsystem output frequency is to operate at 2.01 GHz. Our example crystal frequency is f_{xtal} = *50 MHz, R=1, and m=0 (*Figure 31*)*, hence T_{FSM} = 20 ns (50 MHz). Note, when using AutoCal, the maximum AutoCal Finite State Machine (FSM) clock cannot exceed 60 MHz (see Reg 0Ah*[14:13]*). The FSM clock does not affect the accuracy of the measurement, it only affects the time to produce the result. This same clock is used to clock the 16 bit VCO serial port.

If time to change frequencies is not a concern, then one may set the calibration time for maximum accuracy, and therefore not be concerned with measurement resolution.

Using an input crystal of 50 MHz (R=1 and fpd=50 MHz) the times and accuracies for calibration using (EQ 6) and (EQ 8) are shown in Table 1. Where minimal tuning time is 1/8th of the VCO band spacing.

Across all VCOs, a measurement resolution better than 800 kHz will produce correct results. Setting m = 0, n = 5, provides 781 kHz of resolution and adds 8.6 µs of AutoCal time to a normal frequency hop. Once the AutoCal sets the final switch value, 8.64 µs after the frequency change command, the fractional register will be loaded, and the loop will lock with a normal transient predicted by the loop dynamics. Hence we can see in this example that AutoCal typically adds about 8.6 µs to the normal time to achieve frequency lock. Hence, AutoCal should be used for all but the most extreme frequency hopping requirements.

Table 1. AutoCal Example with F_{xtal} = 50 MHz, R = 1, m = 0

Control Value *Reg0Ah[2:0]*	n	2^n	T_{mmt} (µs)	T_{cal} (µs)	F_{err} Max
0	0	1	0.02	4.92	± 25 MHz
1	1	2	0.04	5.04	± 12.5 MHz
2	2	4	0.08	5.28	± 6.25 MHz
3	3	8	0.16	5.76	± 3.125 MHz
4	5	32	0.64	8.64	± 781 kHz
5	6	64	1.28	12.48	± 390 kHz
6	7	128	2.56	20.16	± 195 kHz
7	8	256	5.12	35.52	± 98 kHz

1.2.5 VCO Output Mute Function

The output mute function enables the HMC833LP6GE to disable the VCO output while maintaining the PLL and VCO subsystems fully functional. The mute function provides over 40 dB of isolation throughout the operating range of the HMC833LP6GE. To mute the output of the HMC833LP6GE, the following register writes are necessary:

1. Initially, and only once, typically after power-up, pre-configure the VCO subsystem by writing VCO_Reg 01h[8:0] = 3h (accomplished by writing to Reg 05h = 188h). This write effectively enables the master enable, and PLL buffer enable, and disables the manual mode RF buffer, divide-by 1, and RF divider of the VCO subsystem, as shown in Figure 27. Although this write disables the manual mode

enables of the VCO subsystem, it has no affect on the PLL or VCO subsystem because typically and by default the VCO subsystem is operating in auto mode.

2. Then to mute the PLL output simply write VCO_Reg 03h [2] = 1 (accomplish by writing to PLL Reg 05h = 2A18h in doubler mode, and Reg 05h = 2A98h in fundamental mode of the VCO), which effectively places the VCO subsystem in manual mode. Manual mode enables have been pre-configured in step 1 to mute the PLL output.
3. If it is required to tune the HMC833LP6GE while the output is muted a final write, Reg 05h = 0h, is required.

To enable the HMC833LP6GE output after muting:

1. Write VCO_Reg 03h [2] = 0 (accomplish by writing to PLL Reg 05h = 2818h in doubler mode, or Reg 05h = 2898h in fundamental mode).
2. A final write to Reg 05h = 0h is required.

Please refer to Figure 27 for more information. Also note that the VCO subsystem registers are not directly accessible. They are written to the VCO subsystem via PLL Reg 05h. More information about VCO subsystem SPI in section 1.19.

1.3 VCO Built in Test with AutoCal

The frequency limits of the VCO can be measured using the BIST features of the AutoCal machine.

This is done by setting Reg 0Ah[10]=1 which freezes the VCO switches in one position. VCO switches may then be written manually, with the varactor biased at the nominal mid-rail voltage used for AutoCal. For example to measure the VCO maximum frequency use switch 0, written to the VCO subsystem via Reg 05h=[000000000 0000 VCOID]. Where VCOID = '000'b.

If AutoCal is enabled, (Reg 0Ah[11] = 0), and a new frequency is written, AutoCal will run, but with switches frozen. The VCO frequency error relative to the command frequency will be measured and results written to Reg 11h[19:0] where Reg 11h[19] is the sign bit. The result will be written in terms of VCO count error (EQ 4). For example if the expected VCO is 2 GHz, reference is 50 MHz, and n is 6, we expect to measure 2560 counts. If we measure a difference of -5 counts in Reg 11h, then it means we actually measured 2555 counts. Hence the actual frequency of the VCO is 5/2560 low, or 1.99609375 GHz, ±1 Count ~ ±781 kHz.

1.4 Spurious Performance

1.4.1 Integer Operation and Reference Spurious

The VCO always operates at an integer multiple of the PD frequency in an integer synthesizer. In general, spurious signals originating from an integer synthesizer can only occur at multiples of the PD frequency. These unwanted outputs closest to the carrier are often simply referred to as reference sidebands. Unwanted reference harmonics can also exist far from the carrier due to circuit isolation.

Spurs unrelated to the reference frequency must originate from outside sources. External spurious sources can modulate the VCO indirectly through power supplies, ground, or output ports, or bypass the loop filter due to poor isolation of the filter. It can also simply add to the output of the PLL.

Reference spurious levels are typically below -100 dBc with a well designed board layout. A regulator with low noise and high power supply rejection, such as the HMC1060LP3E, is recommended to minimize external spurious sources.

Reference spurious levels of below -100 dBc require superb board isolation of power supplies, isolation of the VCO from the digital switching of the synthesizer and isolation of the VCO load from the synthesizer. Typical board layout, regulator design, eval boards and application information are available for very low spurious operation. Operation with lower levels of isolation in the application circuit board, from those recommended by Hittite, can result in higher spurious levels.

If the application environment contains other interfering frequencies unrelated to the PD frequency, and if the application isolation from the board layout and regulation are insufficient, the unwanted interfering frequencies will mix with the desired synthesizer output and cause additional spurious emissions. The level of these emissions is dependant upon isolation and supply regulation or rejection (PSRR).

1.4.2 Fractional Operation and Spurious

Unlike an integer PLL, spurious signals in a fractional PLL can occur due to the fact that the VCO operates at frequencies unrelated to the PD frequency. Hence intermodulation of the VCO and the PD harmonics can cause spurious sidebands. Spurious emissions are largest when the VCO operates very close to an integer multiple of the PD. When the VCO operates exactly at a harmonic of the PD then, no in-close mixing products are present.

As shown in Figure 32, interference is always present at multiples of the PD frequency, f_{pd}, and the VCO frequency, f_{vco}. The difference, Δ, between the VCO frequency and the nearest harmonic of the reference, will create what are referred to as integer boundary spurs. Depending upon the mode of operation of the synthesizer, higher order, lower power spurs may also occur at multiples of integer fractions (sub-harmonics) of the PD frequency. That is, fractional VCO frequencies which are near $nf_{pd} + f_{pd}d/m$, where n, d and m are all integers and d<m (mathematicians refer to d/m as a rational number). We will refer to $f_{pd}d/m$ as an integer fraction. The denominator, m, is the order of the spurious product. Higher values of m produce smaller amplitude spurious at offsets of mΔ and usually when m>4 spurs are small or unmeasurable.

The worst case, in fractional mode, is when d=0, and the VCO frequency is offset from nf_{pd} by less than the loop bandwidth. This is the “in-band integer boundary” case.

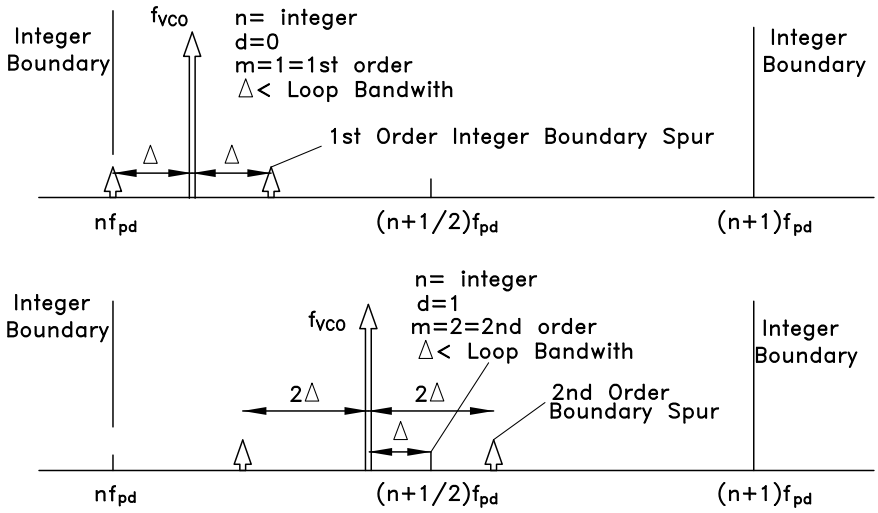


Figure 36. Fractional Spurious Example

Characterization of the levels and orders of these products is not unlike a mixer spur chart. Exact levels of the products are dependent upon isolation of the various synthesizer parts. Hittite can offer guidance about expected levels of spurious with HMC833LP6GE evaluation boards. Regulators with high power supply rejection ratios (PSRR) are recommended, especially in noisy applications.

1.4.2.1 Charge Pump and Phase Detector Spurious Considerations

Charge pump and phase detector linearity are of paramount importance when operating in fractional mode. Any non-linearity degrades phase noise and spurious performance.

We define zero phase error when the reference signal and the divider VCO signal arrive at the Phase Detector at the same time. Phase detector linearity degrades when the phase error is very small and when the random phase errors cause the phase detector to switch back an forth between reference lead and VCO lead.

These switching non-linearities in fractional mode are eliminated by operating the phase detector with an average phase offset such that either the reference or VCO always leads.

A programmable charge pump offset current source is used to add DC current to the loop filter and create the desired phase offset. Positive current causes the VCO to lead, negative current causes the reference to lead.

The offset charge pump is controlled via Reg 09h. The phase offset is scaled from 0 degrees, that is the reference and the VCO path arrive in phase, to 360 degrees, where they arrive a full cycle late. The offset can also be thought of in absolute time difference between the arrivals.

The recommended operating point for the charge pump in fractional mode is one where the time offset at the phase detector is ~2.5ns + $4T_{VCO}$, where T_{VCO} is the RF period at the fractional prescaler input. The required CP offset current should never exceed 25% of the programmed CP current.

The specific level of charge pump offset current Reg 09h[20:14] is determined by this time offset, the comparison frequency and the charge pump current:

$$\text{Required CP Offset} = \min\left[\left(\left(2.5 \bullet 10^{-9} + 4 \bullet T_{VCO}\right)(\text{sec}) \bullet F_{comparison} \bullet I_{CP}\right), 0.25 \bullet I_{CP}\right] \quad \text{(EQ 9)}$$

where:

T_{VCO}*: is the RF period at the fractional prescaler input*

I_{CP}*: is the full scale current setting of the switching charge pump* Reg 09h*[6:0]* Reg 09h*[13:7]*

Operation with charge pump offset influences the required configuration of the Lock Detect function. Refer to the description of Lock Detect function in section 1.11. Note that this calculation can be performed for the center frequency of the VCO, and does not need refinement for small differences < 25 % in center frequencies.

Another factor in the spectral performance in Fractional Mode is the choice of the Delta-Sigma Modulator mode. Mode A can offer better in-band spectral performance (inside the loop bandwidth) while Mode B offers better out of band performance. See Reg 06h[3:2] for DSM mode selection. Finally, all fractional synthesizers create fractional spurs at some level. Hittite offers the lowest level fractional spurious in the industry in an integrated solution.

1.4.2.2 Spurious Related to Channel Step Size (Channel Spurs)

Many fractional PLLs also create spurious emissions at offsets which are multiples of the channel step size. We refer to these as Channel Spurs. It is common in the industry to set the channel step size by use of the so-called modulus. For example, channel step size of 100 kHz requires a small modulus related to the step size, and often results in 100 kHz Channel Spurs.

The HMC833LP6GE uses a large fixed modulus unrelated to the channel step size. As a result, the HMC833LP6GE has extremely low or unmeasurable Channel Spurs. In addition Exact Frequency Mode (1.12.2.2) allows exact channel step size with no Channel Spurs.

The lack of Channel Spurs means that the HMC833LP6GE has large regions of operation between Integer Boundaries with little or no spurs of any kind. Large spurious free zones enable the HMC833LP6GE to be used with a tunable reference, to effectively move the spur free zones and hence achieve spur-free operation at all frequencies. The resulting PLL is virtually spur-free at all frequencies.

For more information see 1.4.2.3.

1.4.2.3 Spurious Reduction with Tunable Reference

Section 1.4.2 discussed fractional mode Integer Boundary spurious caused by VCO operation near reference harmonics. It is possible, with Hittite fractional synthesizers, to virtually eliminate the integer boundary spurious at a given VCO frequency by changing the frequency of the reference. The reference frequency is normally generated by a crystal oscillator and is not tunable. However, Hittite wideband PLLs with Integrated VCOs, including HMC833LP6GE, can be used as a high-quality tunable reference source, as shown in Figure 33.

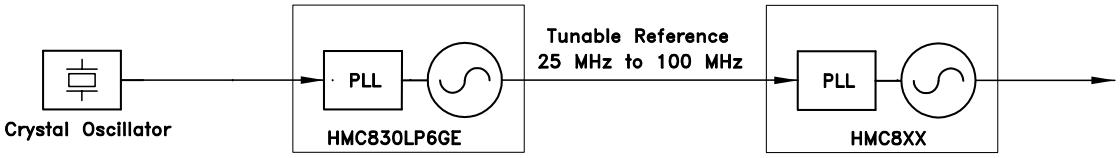


Figure 37. Tunable reference source

With the setup shown in Figure 33, the HMC833LP6GE is capable of operating across all of its frequency range without sacrificing phase noise, while virtually eliminating spurious emissions. Optimum operation requires appropriate configuration of the two synthesizers to achieve this performance. Hittite apps-support can assist with the required algorithms for ultra-low spurious tunable reference applications.

An HMC833LP6GE tunable reference PLL typically uses a high frequency crystal reference for best performance. Phase noise from the MC830LP6GE tunable reference output at 100 kHz offset varies typically from -145 dBc at 100 MHz output to -157 dBc at 25 MHz output. This performance of HMC833LP6GE as a tunable reference is equivalent to the phase noise of high performance crystal oscillators.

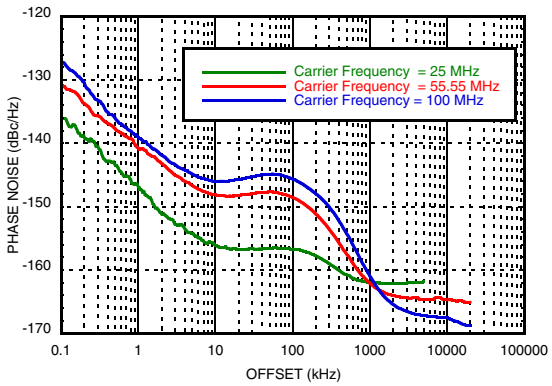


Figure 38. Phase noise performance of the HMC833LP6GE when used with a tunable reference source. (HMC833LP6GE operating at 3 GHz/30, 3 GHz/54, and 1.55 GHz/62 for the 100 MHz, 55.55 MHz, and 25 MHz curves respectively.)

Worst case spurious levels (largest spurs at any offset) of conventional fixed reference vs. a tunable reference can be compared by multiple individual phase noise measurements and summarized on a single plot vs. carrier frequency.

For example, Figure 35 shows the spectrum of a carrier operating at 2000.1 MHz with a 50 MHz fixed reference. This case is 100 kHz away from an Integer Boundary (50 MHz x 40). Worst case spurious can be observed at 100 kHz offset and about -52 dBc in magnitude.

Figure 36 shows the same HMC833LP6GE PLL VCO operating at the same 2000.1 MHz carrier frequency, using a tunable reference at 47.5 MHz generated by HMC830LP6GE. Worst case spurious in this case can be observed at 5 MHz offset and about -100 dBc in magnitude.

The results of Figure 35 and Figure 36 show that the tunable reference source achieves 50 dB better spurious performance, while maintaining essentially the same phase noise performance.

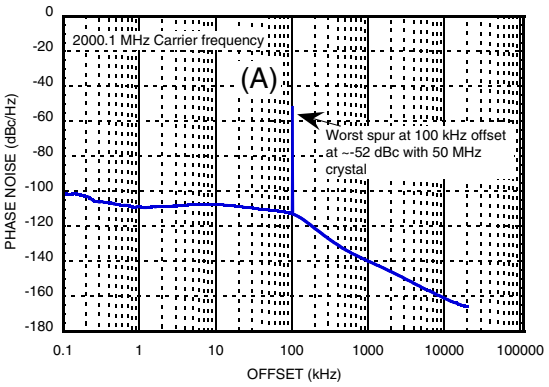


Figure 39. HMC833LP6GE Worst spur at any offset, fixed 50 MHz reference, output frequency = 2000.1 MHz

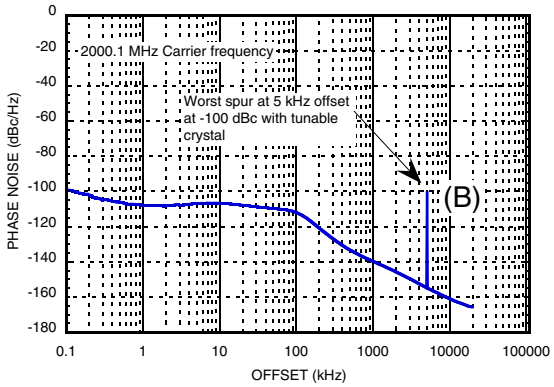


Figure 40. HMC833LP6GE worst spur at any offset, tunable reference (HMC830LP6GE), output frequency = 2000.1 MHz

Many spurious measurements, such as the ones in Figure 35 and Figure 36 can be summarized into a single plot of worst case spurious at any offset vs. carrier frequency as shown in Figure 37. A log frequency display relative to the 2000 MHz fixed reference Integer Boundary was used to emphasize the importance of the loop bandwidth on spurious performance of the fixed reference case. This technique clearly shows the logarithmic roll-off of the worst case spurious when operating near the Integer Boundary. In this case the loop filter bandwidth of the HMC833LP6GE was 100 kHz.

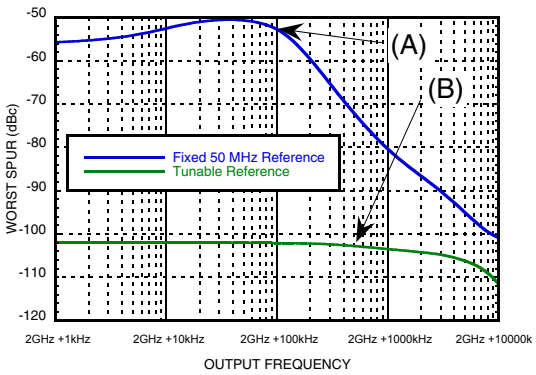


Figure 41. Largest observed spurious, at any offset, using a fixed 50 MHz reference source and a tunable reference source.

For example worst case spurious operating at 2000.1 MHz (point (A)) in Figure 35 with a fixed 50 MHz reference) is represented by a single point in Figure 37 (point (A)) on the blue curve. Similarly, worst case spurious from Figure 36 with variable reference, operating at 2000.1 MHz is represented by a single point in Figure 37 (point (B)) on the green curve.

The plot in Figure 37 is generated by tuning the carrier frequency away from Integer Boundary and recording the worst case spurious, at any offset, at each operating frequency. Figure 37 shows that the worst case spurious for the 50 MHz fixed reference case, is nearly constant between -51 dBc and -55 dBc when operating with a carrier frequency less than 100 kHz from the Integer Boundary (blue curve). It also shows that the worst case spurious rolls off at about 25 dB/decade relative to 1 loop bandwidth. For example, at an operating frequency of 2001 MHz (equivalent to 10 loop bandwidths offset) worst case spurious is -80 dBc. Similarly, at an operating frequency of 2010 MHz (equivalent to 100 loop bandwidths) worst case spurious is -100 dBc.

In contrast, the green curve of Figure 37 shows that the worst case spurious over the same operating frequency range, when using an HMC830LP6GE tunable reference, is below -100 dBc at all operating frequencies!

In general all fractional PLLs have spurious when operating near Integer Boundaries. High performance tunable reference makes it possible to operate HMC833LP6GE, virtually spur-free at all frequencies, with little or no degradation in phase noise.

1.5 Integrated Phase Noise & Jitter

The standard deviation of VCO signal jitter may be estimated with a simple approximation if it is assumed that the locked VCO has a constant phase noise, $\phi^2(f_o)$, at offsets less than the loop 3 dB bandwidth and a 20 dB per decade roll-off at greater offsets. The simple locked VCO phase noise approximation is shown on the left of Figure 38.

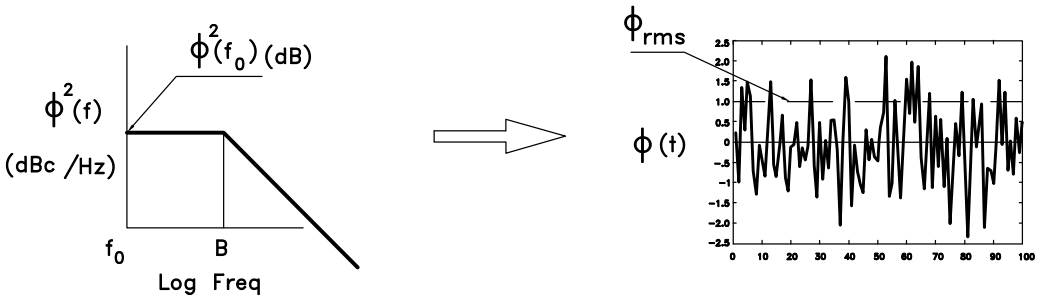


Figure 42. PLL with Integrated VCO Phase Noise & Jitter

With this simplification the total integrated VCO phase noise, ϕ^2, in rads^2 in the linear form is given by

$$\phi^2 = \phi^2(f_o)\, B\pi \qquad \text{(EQ 10)}$$

where $\phi^2(f_o)$ is the single sideband phase noise in rads^2/Hz inside the loop bandwidth, and B is the 3 dB corner frequency of the closed loop PLL

The integrated phase noise at the phase frequency detector, ϕ^2_{pd} is just scaled by N^2

$$\phi^2_{pd} = \phi^2 / N^2 \qquad \text{(EQ 11)}$$

The rms phase jitter of the VCO in rads, ϕ, is just the square root of the phase noise integral.

Since the simple integral of (EQ 10) is just a product of constants, we can easily do the integral in the log domain. For example if the VCO phase noise inside the loop is -100 dBc/Hz at 10 kHz offset and the loop bandwidth is 100 kHz, and the division ratio is 100, then the integrated phase noise at the phase frequency detector, in dB, is given by:

$$\phi^2_{pd\,dB} = 10\log(\phi^2(f_o)B\pi/N^2) = -100 + 50 + 5 - 40 = -85\ dBc$$

or equivalently, $\phi = 10^{-85/20} = 53.6\text{e-}6$ rads = 3.2e-3 degrees.

While the phase noise reduces by a factor of 20logN after division to the reference, due to the increased period of the PD reference signal, the jitter is constant.

The rms jitter from the phase noise is then given by

$$T_{jpn} = T_{pd}\phi_{pd}/2\pi \qquad \text{(EQ 12)}$$

In this example if the PD reference was 50 MHz, T_{pd} = 20ns, and hence T_{jpn} = 179 femto-sec.

It should be noted that this last expression is based upon a closed form integral of the entire spectrum of the oscillator phase noise. This integral starts at DC. It is common for real system to evaluate jitter over

shorter intervals of time, hence the integral often starts at some finite frequency offset and will produce a jitter that is less than that given by the full expression. Finally real oscillators have noise floors that also contribute to jitter. The phase noise of a white noise floor is a simple integral of noise floor density times bandwidth of interest to the system. This additional noise power should be added to the expression of (EQ 16) to give a more accurate jitter number. Depending upon the bandwidth of the system in question this noise floor contribution may be an important factor.

1.6 Reference Input Stage

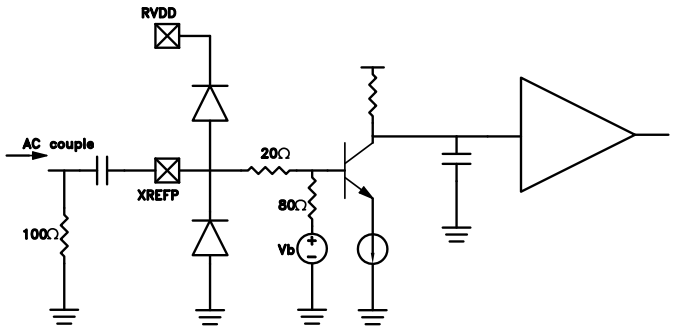


Figure 43. Reference Path Input Stage

The reference buffer provides the path from an external reference source (generally crystal based) to the R divider, and eventually to the phase detector. The buffer has two modes of operation controlled by Reg 08h[21]. High Gain (Reg 08h[21] = 0), recommended below 200 MHz, and High frequency (Reg 08h[21] = 1), for 200 to 350 MHz operation. The buffer is internally DC biased, with 100 Ω internal termination. For 50 Ω match, an external 100 Ω resistor to ground should be added, followed by an AC coupling capacitor (impedance < 1 Ω), then to the XREFP pin of the part.

At low frequencies, a relatively square reference is recommended to keep the input slew rate high. At higher frequencies, a square or sinusoid can be used. The following table shows the recommended operating regions for different reference frequencies. If operating outside these regions the part will normally still operate, but with degraded reference path phase noise performance.

Minimum pulse width at the reference buffer input is 2.5 ns. For best spur performance when R = 1, the pulse width should be (2.5ns + $8T_{PS}$), where T_{PS} is the period of the VCO at the prescaler input. When R > 1 minimum pulse width is 2.5 ns.

Table 2. Reference Sensitivity Table

	Square Input			Sinusoidal Input		
Reference Input Frequency (MHz)	Slew > 0.5V/ns	Recommended Swing (Vpp)			Recommended Power Range (dBm)	
	Recommended	Min	Max	Recommended	Min	Max
< 10	YES	0.6	2.5	x	x	x
10	YES	0.6	2.5	x	x	x
25	YES	0.6	2.5	ok	8	15
50	YES	0.6	2.5	YES	6	15
100	YES	0.6	2.5	YES	5	15
150	ok	0.9	2.5	YES	4	12
200	ok	1.2	2.5	YES	3	8

Input referred phase noise of the PLL when operating at 50 MHz is between -150 and -156 dBc/Hz at 10 kHz offset depending upon the mode of operation. The input reference signal should be 10 dB better than this floor to avoid degradation of the PLL noise contribution. It should be noted that such low levels are only necessary if the PLL is the dominant noise contributor and these levels are required for the system goals.

1.7 Reference Path 'R' Divider

The reference path "R" divider is based on a 14-bit counter and can divide input signals by values from 1 to 16,383 and is controlled by *rdiv (*Reg 02h*).*

Minimum pulse width at the reference buffer input is 2.5 ns. For best spur performance when R = 1, the pulse width should be (2.5 ns + 8Tps), where Tps is the period of the VCO at the prescaler input. When R > 1 minimum pulse width is 2.5 ns.

1.8 RF Path 'N' Divider

The main RF path divider is capable of average divide ratios between 2^{19}-5 (524,283) and 20 in fractional mode, and 2^{19}-1 (524,287) to 16 in integer mode. The VCO frequency range divided by the minimum N divider value will place practical restrictions on the maximum usable PD frequency. For example a VCO operating at 1.5 GHz in fractional mode with a minimum N divider value of 20 will have a maximum PD frequency of 75 MHz.

1.9 Charge Pump & Phase Detector

The Phase detector (PD) has two inputs, one from the reference path divider and one from the RF path divider. When in lock these two inputs are at the same average frequency and are fixed at a constant average phase offset with respect to each other. We refer to the frequency of operation of the PD as f_{pd}. Most formulae related to step size, delta-sigma modulation, timers etc., are functions of the operating frequency of the PD, f_{pd}. f_{pd} is also referred to as the comparison frequency of the PD.

The PD compares the phase of the RF path signal with that of the reference path signal and controls the charge pump output current as a linear function of the phase difference between the two signals. The output current varies linearly over a full ±2π radians (±360°) of input phase difference.

1.10 Phase Detector Functions

Phase detector register Reg 0Bh allows manual access to control special phase detector features.

PD_up_en (Reg 0Bh*[5]), if 0,* masks the PD up output, which prevents the charge pump from pumping up.`

PD_dn_en (Reg 0Bh*[6]), if 0,* masks the PD down output, which prevents the charge pump from pumping down.

Clearing both *PD_up_en* and *PD_dn_en* effectively tri-states the charge pump while leaving all other functions operating internally.

PD Force UP Reg 0Bh*[9] = 1* and PD Force DN Reg 0Bh*[10] = 1* allows the charge pump to be forced up or down respectively. This will force the VCO to the ends to the tuning range which can be useful in test of the VCO.

1.11 Phase Detector Window Based Lock Detect

Lock Detect Enable Reg 07h*[3]=1* is a global enable for all lock detect functions.

The window based Lock Detect circuit effectively measures the difference between the arrival of the reference and the divided VCO signals at the PD. The arrival time difference must consistently be less than the Lock Detect window length, to declare lock. Either signal may arrive first, only the difference in arrival times is counted.

1.11.1 Analog Window Lock Detect

The lock detect window may be generated by either an analog one shot circuit or a digital one shot based upon an internal timer. Setting Reg 07h[6]=0 will result in a fixed, analog, nominal 10 ns window, as shown in Figure 40. The analog window cannot be used if the PD rate is above 50 MHz, or if the offset is too large.

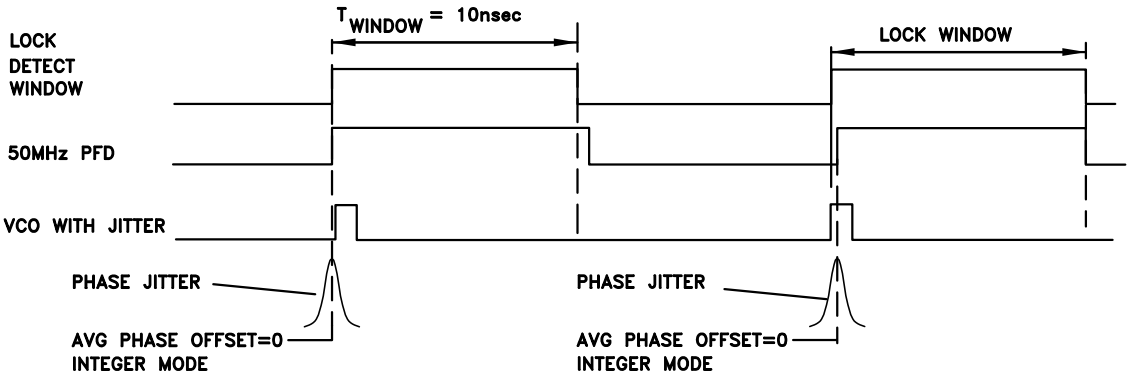


Figure 44. Normal Lock Detect Window - Integer Mode, Zero Offset

For example a 25 MHz PD rate with a 1 mA charge pump setting *(*Reg 09h*[6:0]*=Reg 09h*[13:7]= 32h)* and 400 µA offset down current *(*Reg 09h*[20:14]=50h* Reg 09h*[22]= 1)*, would have an offset of about 400/1000 = 40% of the PD period or about 16 ns. In such an extreme case the divided VCO would arrive 16 ns after the PD reference, and would always arrive outside of the 10 ns lock detect window. In such a case the lock detect circuit would always read unlocked, even though the VCO might be locked. When using the 10 ns analog lock detect window, with a 40 ns PD period, the offset must always be less than 25% of the charge pump setting, 20% to allow for tolerances. Hence a 1 mA charge pump setting can not use more than 200 µA offset with a 25 MHz PD and an analog Lock detect window. Charge pump current, charge pump offset, phase detector rate and lock detect window are related.

1.11.2 Digital Window Lock Detect

Setting Reg 07h*[6]=1* will result in a variable length lock detect window based upon an internal digital timer. The timer period is set by the number of cycles of the internal LD clock as programmed by Reg 07h[9:7]. The LD clock frequency is adjustable by Reg 07h[11:10]. The LD clock signal can be viewed via the GPO test pins. Refer 1.16 for details.

1.11.3 Declaration of Lock

wincnt_max in Reg 07h*[2:0]* defines the number of consecutive counts of the divided VCO that must land inside the lock detect window to declare lock. If for example we set *wincnt_max* = 2048, then the VCO arrival would have to occur inside the window 2048 times in a row to be declared locked, which would result in a Lock Detect Flag high. A single occurrence outside of the window will result in an out of lock, i.e. Lock Detect Flag low. Once low, the Lock Detect Flag will stay low until the *wincnt_max* = 2048 condition is met again.

The Lock Detect Flag status is always readable in Reg 12h*[1]*, if locked = 1. Lock Detect status is also output to the LD_SDO pin if Reg 0Fh*[4:0]=1*. Again, if locked, LD_SDO will be high. Setting Reg 0Fh*[6]=0* will display the Lock Detect Flag on LD_SDO except when a serial port read is requested, in which case the pin reverts temporarily to the Serial Data Out pin, and returns to the Lock Detect Flag after the read is completed. Refer to 1.11.5 for Timing of the Lock Detect information.

1.11.4 Phase Offset & Fractional Linearity

When operating in fractional mode the linearity of the charge pump and phase detector are much more critical than in integer mode. The phase detector linearity is degraded when operating with zero phase offset. Hence in fractional mode it is necessary to offset the phase of the PD reference and the VCO at the phase detector. In such a case, for example with an offset delay, as shown in Figure 41, the VCO arrival will always occur after the reference. The lock detect circuit window may need to be adjusted to allow for the delay being used. for details see section "Digital Lock Detect with Digital Window Example".

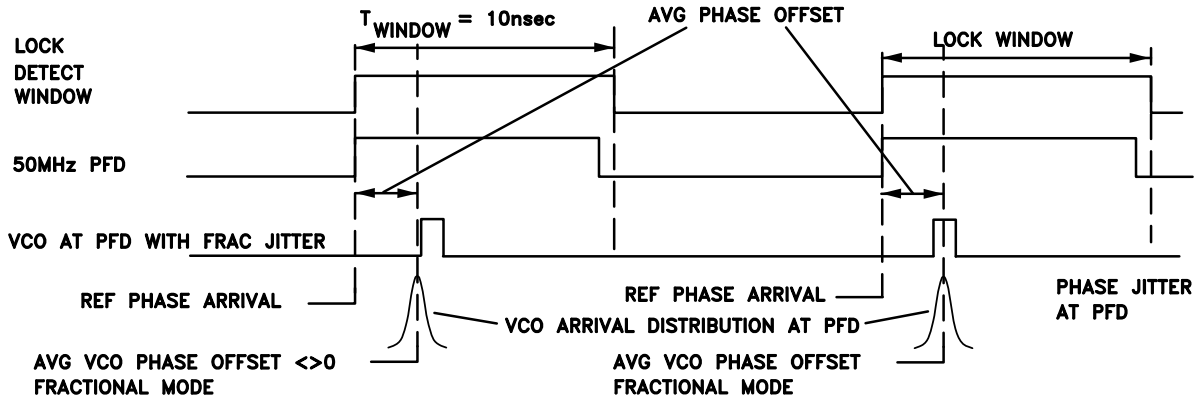


Figure 45. Lock Detect Window - Fractional Mode with Offset

1.11.5 Digital Lock Detect with Digital Window Example

Typical Digital Lock detect window widths are shown in Table 3. Lock Detect windows typically vary ±10% vs voltage and ±25% over temperature (-40°C to +85°C).

Table 3. Typical Digital Lock Detect Window

LD Timer Speed Reg07[11:10]	Digital Lock Detect Window Nominal Value ±25% (ns)							
Fastest 00	6.5	8	11	17	29	53	100	195
01	7	8.9	12.8	21	36	68	130	255
10	1.7	9.2	13.3	22	38	72	138	272
Slowest 11	7.6	10.2	15.4	26	47	88	172	338
LD Timer Divide Setting Reg07[9:7]	0	1	2	3	4	5	6	7
LD Timer Divide Value	0.5	1	2	4	8	16	32	64

As an example, in fractional mode, with a 50 MHz PD, with a Charge pump gain of 2 mA and a Down Leakage of -400 µA (Reg 09h[13:7] = 64h, Reg 09h[6:0] = 64h, Reg 09h[20:14] = 50h, Reg 09h[22] = 1), the average offset at the PD will be -0.400/2 = 0.2 of the PD period, or about 4 ns ±25%. Hence, when in lock, the divided VCO will arrive at the PD about 4 ns after the divided Reference. The Lock Detect Window always starts on the arrival of the first signal at the PD, in this case the Reference. The Lock Detect window must be longer than 4 ns + 25% and shorter than the period of the PD, in this example, 20 ns. A perfect Lock Detect window would be the geometric mean or 9.8 ns.

A comfortable solution of 12.8 ns with timer speed set at Reg 07h*[11:10]=1* and Timer divider Reg 07h*[9:7]=2* works well for the example PD frequency and charge pump offset setting.

Tolerance on the window is +25% at +85 °C, -25% at -40 °C. Here 12.8 ns nominal window may extend by +25% at +85°C to 16 ns, which is fine for a PD period of 20 ns. Also the minimum window may shrink by 25% to 9.6 ns at -40°C, which again works well for the worst case offset of 4.6 ns.

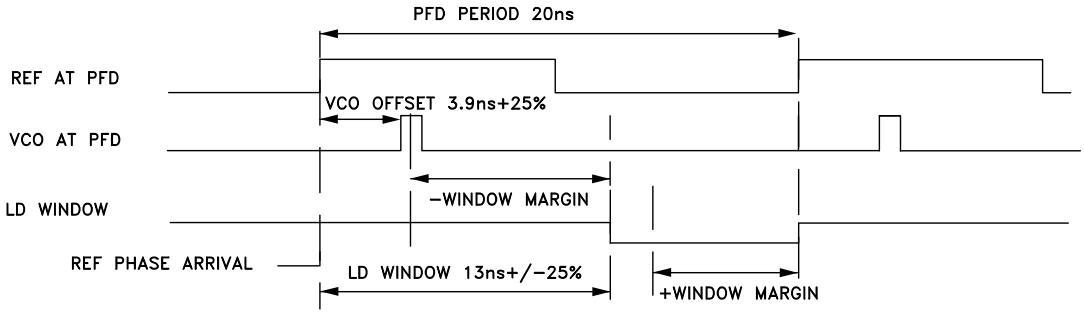


Figure 46. Lock Detect Window Example with 50 MHz PD and 3.9 ns VCO Offset

There is always a good solution for the lock detect window for a given operating point. The user should understand however that one solution does not fit all operating points. If charge pump offset or PD frequency are changed significantly then the lock detect window may need to be adjusted.

1.11.6 Cycle Slip Prevention (CSP)

When changing VCO frequency and the VCO is not yet locked to the reference, the instantaneous frequencies of the two PD inputs are different, and the phase difference of the two inputs at the PD varies rapidly over a range much greater than ±2π radians. Since the gain of the PD varies linearly with phase up to ±2π, the gain of a conventional PD will cycle from high gain, when the phase difference approaches a multiple of 2π, to low gain, when the phase difference is slightly larger than a multiple of 0 radians. The output current from the charge pump will cycle from maximum to minimum even though the VCO has not yet reached its final frequency.

The charge on the loop filter small cap may actually discharge slightly during the low gain portion of the cycle. This can make the VCO frequency actually reverse temporarily during locking. This phenomena is known as cycle slipping. Cycle slipping causes the pull-in rate during the locking phase to vary cyclically. Cycle Slipping increases the time to lock to a value greater than that predicted by normal small signal Laplace analysis.

The synthesizer PD features an ability to reduce cycle slipping during acquisition. The Cycle Slip Prevention (CSP) feature increases the PD gain during large phase errors. The specific phase error that triggers the momentary increase in PD gain is set via Reg 0Bh[8:7]

1.11.7 Charge Pump Gain

A simplified diagram of the charge pump is shown in Figure 43. Charge pump Up and Down gains are set by *CP DN Gain* and *CP UP Gain* respectively *(*Reg 09h*[6:0] and* Reg 09h *[13:7])*. The current gain of the pump in Amps/radian is equal to the gain setting of this register divided by 2π.

For example if both *CP DN Gain* and *CP UP Gain* are set to '50d' the output current of each pump will be 1 mA and the phase frequency detector gain k_p = 1 mA/2π radians, or 159 µA/rad. See section 1.4 for more information.

1.11.8 Charge Pump Phase Offset - Fractional Mode

In integer mode, the phase detector operates with zero offset. The divided reference signal and the divided VCO signal arrive at the phase detector inputs at the same time. In fractional mode of operation, charge pump linearity and ultimately, phase noise, is much better if the VCO and reference inputs are operated

with a phase offset. A phase offset is implemented by adding a constant DC offset current at the output of the charge pump.

DC offset may be added to the UP or DN switching pumps using Reg 09h*[21] or* Reg 09h*[22]*. The magnitude of the offset is controlled by Reg 09h[20:14], and can range from 0 to 635 µA in steps of 5 µA. Down offset is highly recommended in fractional mode of operation. Integer mode of operation works best with zero offset.

As an example, a PD comparison of f_{PD} = 50 MHz (20 ns period) with the main pump gain set at 2 mA, and a down (DN) offset of -385 µA would represent a phase offset of about (-385/2000)*360 = -69 degrees. This is equivalent to the divided VCO arriving 3.8 ns after the reference at the PD input. It is critical that phase offset be used in fractional mode. Normally, down offsets larger than 3 ns are typical.

If the charge pump gain is changed, for example to compensate for changes in VCO sensitivity, it is recommended to change the charge pump offset proportionally to maintain a constant phase offset.

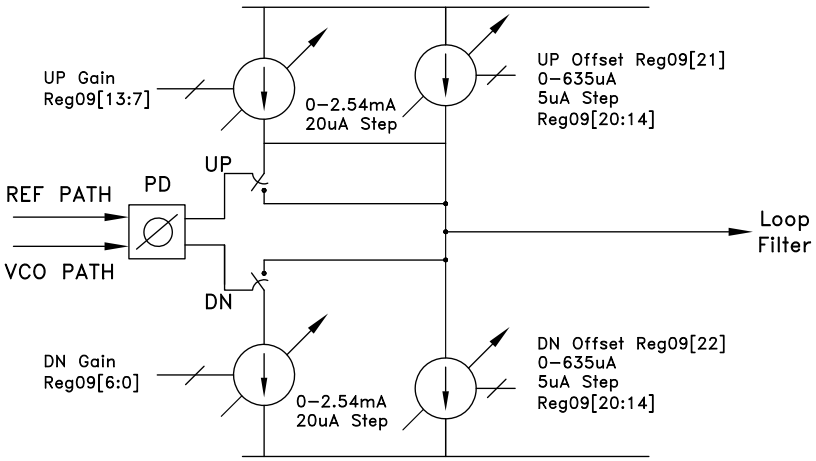


Figure 47. Charge Pump Gain & Offset Control

1.12 Frequency Tuning

HMC833LP6GE VCO subsystem always operates in fundamental frequency of operation (1500 MHz to 3000 MHz). The HMC833LP6GE generates frequencies below its fundamental frequency (25 MHz to 1500 MHz) by tuning to the appropriate fundamental frequency and selecting the appropriate Output Divider setting (divide by 2/4/6.../60/62) in VCO_Reg 02h[5:0]. Conversely the HMC833LP6GE generates frequencies greater than its fundamental frequency (3000 MHz to 6000 MHz) by tuning to the appropriate fundamental frequency and enabling the doubler mode (VCO_Reg 03h [0] = 1).

The HMC833LP6GE automatically controls frequency tuning in the fundamental band of operation, for more information see "1.2.1 VCO Auto-Calibration (AutoCal)".

To tune to frequencies below the fundamental frequency range (<1500 MHz) it is required to tune the HMC833LP6GE to the appropriate fundamental frequency, then select the appropriate output divider setting (divide by 2/4/6.../60/62) in VCO_Reg 02h[5:0]. Similarly, to tune to frequencies above the fundamental frequency range (> 3000 MHz) it is required to tune the HMC833LP6GE to the appropriate fundamental frequency, and then enable the doubler mode of operation (VCO_Reg 03h [0] = 1).

1.12.1 Integer Mode

The HMC833LP6GE is capable of operating in integer mode. For Integer mode set the following registers

a. Disable the Fractional Modulator, Reg 06h*[11]=0*

b. Bypass the Modulator circuit, Reg 06h*[7]=1*

In integer mode the VCO step size is fixed to that of the PD frequency, f_{pd}. Integer mode typically has 3 dB lower phase noise than fractional mode for a given PD operating frequency. Integer mode, however, often requires a lower PD frequency to meet step size requirements. The fractional mode advantage is that higher PD frequencies can be used, hence lower phase noise can often be realized in fractional mode. Charge Pump offset should be disabled in integer mode.

1.12.1.1 Integer Frequency Tuning

In integer mode the digital ΔΣ modulator is shut off and the N (Reg 03h) divider may be programmed to any integer value in the range 16 to 2^{19}-1. To run in integer mode configure Reg 06h as described, then program the integer portion of the frequency as explained by (EQ 13), ignoring the fractional part.

a. Disable the Fractional Modulator, Reg 06h[11] = 0
b. Bypass the delta-sigma modulator Reg 06h[7] = 1
c. To tune to frequencies (<1500 MHz), select the appropriate output divider value VCO_Reg 02h[5:0].
d. To tune to frequencies (>3000 MHz), enable the doubler mode of operation (VCO_Reg 03h [0] = 1).

Writing to VCO subsystem registers (VCO_Reg 02h[5:0] and VCO_Reg 03h [0] in this case) is accomplished indirectly through PLL register 5 (Reg 05h). More information on communicating with the VCO subsystem through PLL Reg 05h is available in "1.19 VCO Serial Port Interface (SPI)" section.

1.12.2 Fractional Mode

The HMC833LP6GE is placed in fractional mode by setting the following registers:

a. Enable the Fractional Modulator, Reg 06h*[11]=1*
b. Connect the delta sigma modulator in circuit, Reg 06h*[7]=0*

1.12.2.1 Fractional Frequency Tuning

This is a generic example, with the goal of explaining how to program the output frequency. Actual variables are dependant upon the reference in use.

The HMC833LP6GE in fractional mode can achieve frequencies at fractional multiples of the reference. The frequency of the HMC833LP6GE, f_{vco}, is given by

$$f_{vco} = \frac{f_{xtal}}{R}\ (N_{int} + N_{frac}) = f_{int} + f_{frac} \qquad \text{(EQ 13)}$$

$$f_{out} = f_{vco} / k \qquad \text{(EQ 14)}$$

Where:

f_{out}	is the output frequency after any potential dividers or doublers.
k	is 0.5 for doubler, 1 for fundamental, or k = 1,2,4,6,…58,60,62 according to the VCO Subsystem type
N_{int}	is the integer division ratio, Reg 03h, an integer number between 20 and 524,284
N_{frac}	is the fractional part, from 0.0 to 0.99999...,N_{frac}=Reg 04h/2^{24}
R	is the reference path division ratio, Reg 02h

f_{xtal}	is the frequency of the reference oscillator input
f_{pd}	is the PD operating frequency, f_{xtal}/R

As an example:

f_{out}	1402.5 MHz
k	2
f_{vco}	2,805 MHz
f_{xtal}	= 50 MHz
R	= 1
f_{pd}	= 50 MHz
N_{int}	= 56
N_{frac}	= 0.1
Reg 04h	= round(0.1 x 2^{24}) = round(1677721.6) = 1677722

$$f_{VCO} = \frac{50e6}{1}\left(56 + \frac{1677722}{2^{24}}\right) = 2805\ MHz + 1.92\ Hz\ error \quad \text{(EQ 15)}$$

$$f_{out} = \frac{f_{VCO}}{2} = 1402.5\ MHz + 0.596\ Hz\ error \quad \text{(EQ 16)}$$

In this example the output frequency of 1402.5 MHz is achieved by programming the 19-bit binary value of 56d = 38h into *intg_reg* in Reg 03h, and the 24-bit binary value of 1677722d = 19999Ah into *frac_reg* in Reg 04h. The 0.596 Hz quantization error can be eliminated using the exact frequency mode if required. In this example the output fundamental is divided by 2. Specific control of the output divider is required. See section 3.0 and description for more details.

1.12.2.2 Exact Frequency Tuning

Due to quantization effects, the absolute frequency precision of a fractional PLL is normally limited by the number of bits in the fractional modulator. For example, a 24 bit fractional modulator has frequency resolution set by the phase detector (PD) comparison rate divided by 2^{24}. The value 2^{24} in the denominator is sometimes referred to as the modulus. Hittite PLLs use a fixed modulus which is a binary number. In some types of fractional PLLs the modulus is variable, which allows exact frequency steps to be achieved with decimal step sizes. Unfortunately small steps using small modulus values results in large spurious outputs at multiples of the modulus period (channel step size). For this reason Hittite PLLs use a large fixed modulus. Normally, the step size is set by the size of the fixed modulus. In the case of a 50 MHz PD rate, a modulus of 2^{24} would result in a 2.98 Hz step resolution, or 0.0596 ppm. In some applications it is necessary to have exact frequency steps, and even an error of 3 Hz cannot be tolerated.

Fractional PLLs are able to generate exact frequencies (with zero frequency error) if N can be exactly represented in binary (eg. N = 50.0,50.5,50.25,50.75 etc.). Unfortunately, some common frequencies cannot be exactly represented. For example, N_{frac} = 0.1 = 1/10 must be approximated as round((0.1 x 2^{24})/ 2^{24}) ≈ 0.100000024. At f_{PD} = 50 MHz this translates to 1.2 Hz error. Hittite's exact frequency mode addresses this issue, and can eliminate quantization error by programming the channel step size to F_{PD}/10 in Reg 0Ch to 10 (in this example). More generally, this feature can be used whenever the desired frequency, f_{VCO}, can be exactly represented on a step plan where there are an integer number of steps (<2^{14}) across integer-N boundaries. Mathematically, this situation is satisfied if:

$$f_{VCOk} \bmod\left(f_{gcd}\right) = 0 \quad \text{where} f_{gcd} = \gcd(f_{VCO1}, f_{PD}) \text{and} f_{gcd} \geq \left(\frac{f_{PD}}{2^{14}}\right) \qquad \text{(EQ 17)}$$

Where:

gcd stands for Greatest Common Divisor

f_N = maximum integer boundary frequency < f_{VCO1}

f_{PD} = frequency of the Phase Detector

and f_{VCOk} are the channel step frequencies where $0 < k < 2^{24}-1$, As shown in Figure 44.

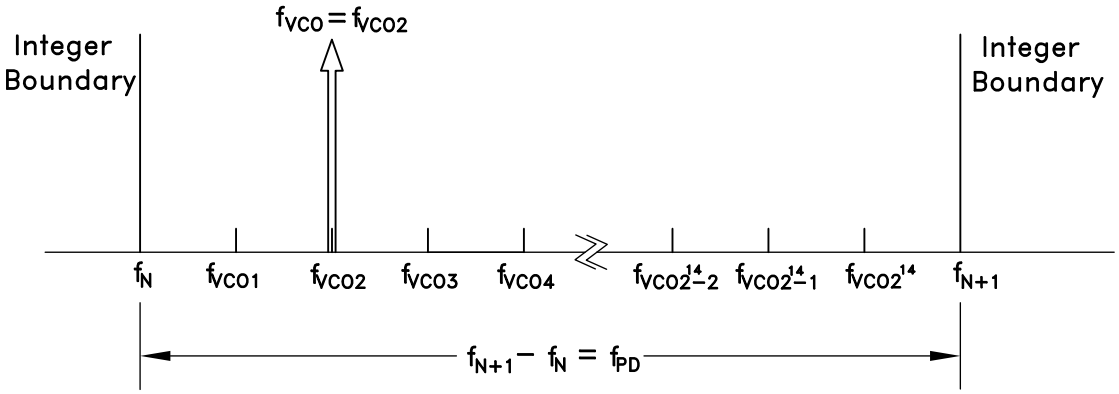


Figure 48. Exact Frequency Tuning

Some fractional PLLs are able to achieve this by adjusting (shortening) the length of the Phase Accumulator (the denominator or the modulus of the Delta-Sigma modulator) so that the Delta-Sigma modulator phase accumulator repeats at an exact period related to the interval frequency (f_{VCOk} - $f_{VCO(k-1)}$) in Figure 44. Consequently, the shortened accumulator results in more frequent repeating patterns and as a result often leads to spurious emissions at multiples of the repeating pattern period, or at harmonic frequencies of f_{VCOk} - $f_{VCO(k-1)}$. For example, in some applications, these intervals might represent the spacing between radio channels, and the spurious would occur at multiples of the channel spacing.

The Hittite method on the other hand is able to generate exact frequencies between adjacent integer-N boundaries while still using the full 24 bit phase accumulator modulus, thus achieving exact frequency steps with a high phase detector comparison rate, which allows Hittite PLLs to maintain excellent phase noise and spurious performance in the Exact Frequency Mode.

1.12.2.3.3 Using Hittite Exact Frequency Mode

If the constraint in (EQ 17) is satisfied, HMC833LP6GE is able to generate signals with zero frequency error at the desired VCO frequency. Exact Frequency Mode may be re-configured for each target frequency, or be set-up for a fixed f_{gcd} which applies to all channels.

1.12.2.4.4 Configuring Exact Frequency Mode For a Particular Frequency

1. Calculate and program the integer register setting Reg 03h = N_{INT} = floor(f_{VCO}/f_{PD}), where the floor function is the rounding down to the nearest integer. Then the integer boundary frequency $f_N = N_{INT} \cdot f_{PD}$
2. Calculate and program the exact frequency register value Reg 0Ch = f_{PD}/f_{gcd}, where f_{gcd} = gcd(f_{VCO},f_{PD})
3. Calculate and program the fractional register setting Reg 04h $= N_{FRAC} = \text{ceil}\left(\frac{2^{24}\left(f_{VCO} - f_N\right)}{f_{PD}}\right)$, where ceil is the ceiling function meaning "round up to the nearest integer."

Example: To configure the HMC833LP6GE for exact frequency mode at f_{VCO} = 2800.2 MHz where Phase Detector (PD) rate f_{PD} = 61.44 MHz Proceed as follows:

Check (EQ 17) to confirm that the exact frequency mode for this f_{VCO} is possible.

$$f_{gcd} = \text{gcd}(f_{VCO}, f_{PD}) \; and \; f_{gcd} \geq \left(\frac{f_{PD}}{2^{14}}\right)$$

$$f_{gcd} = \text{gcd}\left(2800.2\times10^6, 61.44\times10^6\right) = 120\times10^3 > \frac{61.44\times10^6}{2^{14}} = 3750$$

Since (EQ 17) is satisfied, the HMC833LP6GE can be configured for exact frequency mode at f_{VCO} = 2800.2 MHz as follows:

1. N_{INT} = Reg 03h = $floor\left(\frac{f_{VCO}}{f_{PD}}\right) = floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45d = 2Dh$

2. Reg 0Ch = $\frac{f_{PD}}{\text{gcd}\left(f_{VCO}, f_{PD}\right)} = \frac{61.44\times10^6}{\text{gcd}\left(2800.2\times10^6, 61.44\times10^6\right)} = \frac{61.44\times10^6}{120000} = 512d = 200h$

3. To program Reg 04h, the closest integer-N boundary frequency f_N that is less than the desired VCO frequency f_{VCO} must be calculated. $f_N = f_{PD} \cdot N_{INT}$. Using the current example:

$f_N = f_{PD} \times N_{INT} = 45 \times 61.44 \times 10^6 = 2764.8\,MHz.$

Then Reg04h $= ceil\left(\frac{2^{24}\left(f_{VCO} - f_N\right)}{f_{PD}}\right) = ceil\left(\frac{2^{24}\left(2800.2\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9666560d = 938000h$

1.12.2.5.5 Hittite Exact Frequency Channel Mode

If it is desirable to have multiple, equally spaced, exact frequency channels that fall within the same interval (ie. $f_N \leq f_{VCOk} < f_{N+1}$) where f_{VCOk} is shown in Figure 44 and $1 \leq k \leq 2^{14}$, it is possible to maintain the same integer-N (Reg 03h) and exact frequency register (Reg 0Ch) settings and only update the fractional register (Reg 04h) setting. The Exact Frequency Channel Mode is possible if (EQ 17) is satisfied for at least two equally spaced adjacent frequency channels, i.e. the channel step size.

To configure the HMC833LP6GE for Exact Frequency Channel Mode, initially and only at the beginning, integer (Reg 03h) and exact frequency (Reg 0Ch) registers need to be programmed for the smallest f_{VCO} frequency (f_{VCO1} in Figure 44), as follows:

1. Calculate and program the integer register setting Reg 03h = N_{INT} = floor(f_{VCO1}/f_{PD}), where f_{VCO1} is shown in Figure 44 and corresponds to minimum channel VCO frequency. Then the lower integer boundary frequency is given by $f_N = N_{INT} \cdot f_{PD}$.
2. Calculate and program the exact frequency register value Reg 0Ch = f_{PD}/f_{gcd}, where f_{gcd} = gcd((f_{VCOk+1} - f_{VCOk}),f_{PD}) = greatest common divisor of the desired equidistant channel spacing and the PD frequency ((f_{VCOk+1} - f_{VCOk}) and f_{PD}).

Then, to switch between various equally spaced intervals (channels) only the fractional register (Reg 04h) needs to be programmed to the desired VCO channel frequency f_{VCOk} in the following manner:

Reg 04h = $N_{FRAC} = \text{ceil}\left(\frac{2^{24}\left(f_{VCOk} - f_N\right)}{f_{PD}}\right)$ where $f_N = \text{floor}(f_{VCO1}/f_{PD})$, and f_{VCO1}, as shown in Figure 44, represents the smallest channel VCO frequency that is greater than f_N.

Example: To configure the HMC833LP6GE for Exact Frequency Mode for equally spaced intervals of 100 kHz where first channel (Channel 1) = f_{VCO1} = 2800.200 MHz and Phase Detector (PD) rate f_{PD} = 61.44 MHz proceed as follows:

First check that the exact frequency mode for this f_{VCO1} = 2800.2 MHz (Channel 1) and f_{VCO2} = 2800.2 MHz + 100 kHz = 2800.3 MHz (Channel 2) is possible.

$$f_{gcd1} = \gcd(f_{VCO1}, f_{PD}) \; and \; f_{gcd1} \geq \left(\frac{f_{PD}}{2^{14}}\right) \; and \; f_{gcd2} = \gcd(f_{VCO2}, f_{PD}) \; and \; f_{gcd2} \geq \left(\frac{f_{PD}}{2^{14}}\right)$$

$$f_{gcd1} = \gcd\left(2800.2\times10^6, 61.44\times10^6\right) = 120\times10^3 > \frac{61.44\times10^6}{2^{14}} = 3750$$

$$f_{gcd2} = \gcd\left(2800.3\times10^6, 61.44\times10^6\right) = 20\times10^3 > \frac{61.44\times10^6}{2^{14}} = 3750$$

If (EQ 17) is satisfied for at least two of the equally spaced interval (channel) frequencies $f_{VCO1}, f_{VCO2}, f_{VCO3}, \ldots f_{VCON}$, as it is above, Hittite Exact Frequency Channel Mode is possible for all desired channel frequencies, and can be configured as follows:

1. Reg 03h = $floor\left(\frac{f_{VCO1}}{f_{PD}}\right) = floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45d = 2Dh$
2. Reg 0Ch = $\frac{f_{PD}}{\gcd\left(\left(f_{VCOk+1} - f_{VCOk}\right), f_{PD}\right)} = \frac{61.44\times10^6}{\gcd\left(100\times10^3, 61.44\times10^6\right)} = \frac{61.44\times10^6}{20000} = 3072d = C00h$

   where (f_{VCOk+1} - f_{VCOk}) is the desired channel spacing (100 kHz in this example).
3. To program Reg 04h the closest integer-N boundary frequency f_N that is less than the smallest channel VCO frequency f_{VCO1} must be calculated. f_N = floor(f_{VCO1}/f_{PD}). Using the current example:

   $$f_N = f_{PD} \times floor\left(\frac{2800.2\times10^6}{61.44\times10^6}\right) = 45\times61.44\times10^6 = 2764.8\,MHz$$ Then

   $$\text{Reg 04h} = ceil\left(\frac{2^{24}\left(f_{VCO1} - f_N\right)}{f_{PD}}\right) \text{ for channel 1 where } f_{VCO1} = 2800.2\,MHz$$

   $$= ceil\left(\frac{2^{24}\left(2800.2\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9666560d = 938000h$$
4. To change from channel 1 (f_{VCO1} = 2800.2 MHz) to channel 2 (f_{VCO2} = 2800.3 MHz), only Reg 04h needs to be programmed, as long as all of the desired exact frequencies f_{VCOk} (Figure 44) fall between the same integer-N boundaries ($f_N < f_{VCOk} < f_{N+1}$). In that case

   Reg 04h = $ceil\left(\frac{2^{24}\left(2800.3\times10^6 - 2764.8\times10^6\right)}{61.44\times10^6}\right) = 9693867d = 93EAABh$, and so on.

1.12.2.6 Seed Register & AutoSeed Mode

The start phase of the fractional modulator digital phase accumulator (DPA) may be set to one of four possible default values via the seed register Reg 06h*[1:0]*. If AutoSeed Reg 06h*[8]* is set, then the HMC833LP6GE will automatically reload the start phase into the DPA every time a new fractional frequency is selected.

If AutoSeed is not set, then the HMC833LP6GE will start new fractional frequencies with the last value left in the DPA from the last frequency. Hence the start phase will effectively be random. Certain zero or binary seed values may cause spurious energy correlation at specific frequencies. Correlated spurs are advantageous only in very special cases where the spurious are known to be far out of band and are removed in the loop filter. For most cases a random, or non zero, non-binary start seed is recommended. Further, since the AutoSeed always starts the accumulators at the same place, performance is repeatable if AutoSeed is used. Reg 06h*[1:0]=2* is recommended.

1.13 Soft Reset & Power-On Reset

The HMC833LP6GE features a hardware Power on Reset (POR). All chip registers will be reset to default states approximately 250 µs after power up.

The PLL subsystem SPI registers may also be soft reset by an SPI write to register *rst_swrst (*Reg 00h*)*. Note that the soft reset does not clear the SPI mode of operation referred to in section 1.17.2. It should be noted that the VCO subsystem is not affected by the PLL soft reset, the VCO subsystem registers can only be reset by removing the power supply.

*NOTE: if external power supplies or regulators have rise times slower than 250 µs, then it is advised to write to the SPI reset register (*Reg 00h*[5]=1) immediately after power up, before any other SPI activity. This will ensure starting from a known state.*

1.14 Power Down Mode

Note that the VCO subsystem is not affected by the CEN or soft reset. Hence device power down is a two step process. First power down the VCO by writing 0 to VCO register 1 via Reg 05h and then power down the PLL by pulling CEN pin 17 low (assuming no SPI overrides (Reg 01h[0]=1)). This will result in all analog functions and internal clocks disabled. Current consumption will typically drop below 10 µA in Power Down state. The serial port will still respond to normal communication in Power Down mode.

It is possible to ignore the CEN pin, by clearing *rst_chipen_pin_select (*Reg 01h*[0]=0)*. Control of Power Down Mode then comes from the serial port register *rst_chipen_from_spi,* Reg 01h*[1]* .

It is also possible to leave various blocks on when in Power Down *(see* Reg 01h*)*, including:

a. Internal Bias Reference Sources	Reg 01h*[2]*
b. PD Block	Reg 01h*[3]*
c. CP Block	Reg 01h*[4]*
d. Reference Path Buffer	Reg 01h*[5]*
e. VCO Path buffer	Reg 01h*[6]*
f. Digital I/O Test pads	Reg 01h*[7]*

To turn off the VCO RF buffer but leave the VCO running and the PLL locked write Reg 05h = 2A98(manual select) then write Reg 05h = 0D88(disable VCO RF buffer) To re-enable the RF buffer write Reg 05h=0F88(Enable VCO RF buffer)

1.15 Chip Identification

PLL subsystem version information may be read by reading the content of read only register, chip_ID in Reg 00h. It is not possible to read the VCO subsystem version.

1.16 General Purpose Output (GPO) Pin

The PLL shares the LD_SDO (Lock-Detect/Serial Data Out) pin to perform various functions. While the pin is most commonly used to read back registers from chip via the SPI, it is also capable of exporting a variety of interesting signals and real time test waveforms (including Lock Detect). It is driven by a tri-state CMOS driver with ~200 Ω Rout. It has logic associated with it to dynamically select whether the driver is enabled,

and to decide which data to export from the chip.

In its default configuration, after power-on-reset, the output driver is disabled, and only drives during appropriately addressed SPI reads. This allows it to share the output with other devices on the same bus.

Depending on the SPI mode, the read section of SPI cycle is recognized differently

HMC SPI Mode: The driver is enabled during the last 24 bits of SPI READ cycle (not during write cycles).

Open SPI Mode: The driver is enabled if the chip is addressed - ie. The last 3 bits of SPI cycle = '000'b before the rising edge of SEN (Note A).

To monitor any of the GPO signals, including Lock Detect, set Reg 0Fh[7] = 1 to keep the SDO driver always on. This stops the LDO driver from tri-stating and means that the SDO line cannot be shared with other devices.

The chip will naturally switch away from the GPO data and export the SDO during an SPI read (Note B). To prevent this automatic data selection, and always select the GPO signal, set "Prevent AutoMux of SDO" (Reg 0Fh[6] = 1). The phase noise performance at this output is poor and uncharacterized. Also, the GPO output should not be toggling during normal operation. Otherwise the spectral performance may degrade.

Note that there are additional controls available, which may be helpful if sharing the bus with other devices:

- To allow the driver to be active (subject to the conditions above) even when the chip is disabled - set Reg 01h[7] = 0.
- To disable the driver completely, set Reg 08h[5] = 0 (it takes precedence over all else).
- To disable either the pull-up or pull-down sections of the driver, Reg 0Fh[8] = 1 or Reg 0Fh[9] = 1 respectively.

Note A: If SEN rises before SCK has clocked in an 'invalid' (non-zero) chip -address, the HMC833LP6GE will start to drive the bus.

Note B: In Open Mode, the active portion of the read is defined between the 1st SCK rising edge after SEN, to the next rising edge of SEN.

Example Scenarios:

- Drive SDO during reads, tri-state otherwise (to allow bus-sharing)
  - No action required.
- Drive SDO during reads, Lock Detect otherwise
  - Set GPO Select Reg 0Fh[4:0] = '00001' (which is default)
  - Set "Prevent GPO driver disable" (Reg 0Fh[7] = 1)
- Always drive Lock Detect
  - Set " Prevent AutoMux of SDO" Reg 0Fh[6] = 1
  - Set GPO Select Reg 0Fh[4:0]= 00001 (which is default)
  - Set "Prevent GPO driver disable" (Reg 0Fh[7] = 1))

The signals available on the GPO are selected by changing "GPO Select", Reg 0Fh[4:0].

1.17 SERIAL PORT

1.17.1 Serial Port Modes of Operation

The HMC833LP6GE serial port interface can operate in two different modes of operation.

a. HMCSPI HMC Mode (HMC Legacy Mode) - Single slave per HMCSPI Bus

b. HMCSPI Open Mode - Up to 8 slaves per HMCSPI Bus.

Both Modes support 5-bits of register address space. HMC Mode can support up to 6 bits of register

address.

Register 0 has a dedicated function in each mode. Open Mode allows wider compatibility with other manufacturers SPI protocols.

Table 4. Register 0 Comparison - Single vs Multi-User Modes

	Single User HMC Mode	Multi-User Open Mode
READ	Chip ID 24-bits	Chip ID 24-bits
WRITE	Soft Reset, General Strobes	Read Address [4:0] Soft reset [5] General Strobes [23:6]

1.17.2 HMCSPI Protocol Decision after Power-On Reset

On power up both types of modes are active and listening.

A decision to select the desired SPI protocol is made on the first occurrence of SEN or SCLK following a hard reset, after which the protocol is fixed and only changeable by cycling the power OFF and ON.

a. If a rising edge on SEN is detected first HMC Mode is selected.
b. If a rising edge on SCLK is detected first Open mode is selected.

1.17.3 Serial Port HMC Mode - Single PLL

HMC Mode (Legacy Mode) serial port operation can only address and talk to a single PLL, and is compatible with most Hittite PLLs and PLLs with Integrated VCOs.

The HMC Mode protocol, shown in figures Figure 45 and Figure 46, is designed for a 4 wire interface with a fixed protocol featuring

a. 1 Read/Write bit
b. 6 Address bits
c. 24 data bits
d. 3 wire for Write only, 4 wire for Read/Write capability

1.17.3.1 HMC Mode - Serial Port WRITE Operation

AVDD = DVDD = 3V ±10%, AGND = DGND = 0V

Table 5. SPI HMC Mode - Write Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			ns
t_2	SDI to SCLK setup time	3			ns
t_3	SCLK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
t_5	SCK to SEN fall	10			ns
	Max Serial port Clock Speed		50		MHz

A typical HMC Mode WRITE cycle is shown in Figure 45.

a. The Master (host) both asserts SEN (Serial Port Enable) and clears SDI to indicate a WRITE cycle, followed by a rising edge of SCK.
b. The slave (synthesizer) reads SDI on the 1st rising edge of SCK after SEN. SDI low indicates a Write cycle (/WR).
c. Host places the six address bits on the next six falling edges of SCK, MSB first.
d. Slave shifts the address bits in the next six rising edges of SCK (2-7).

e. Host places the 24 data bits on the next 24 falling edges of SCK, MSB first.
f. Slave shifts the data bits on the next 24 rising edges of SCK (8-31).
g. The data is registered into the chip on the 32nd rising edge of SCK.
h. SEN is cleared after a minimum delay of t_5. This completes the write cycle.

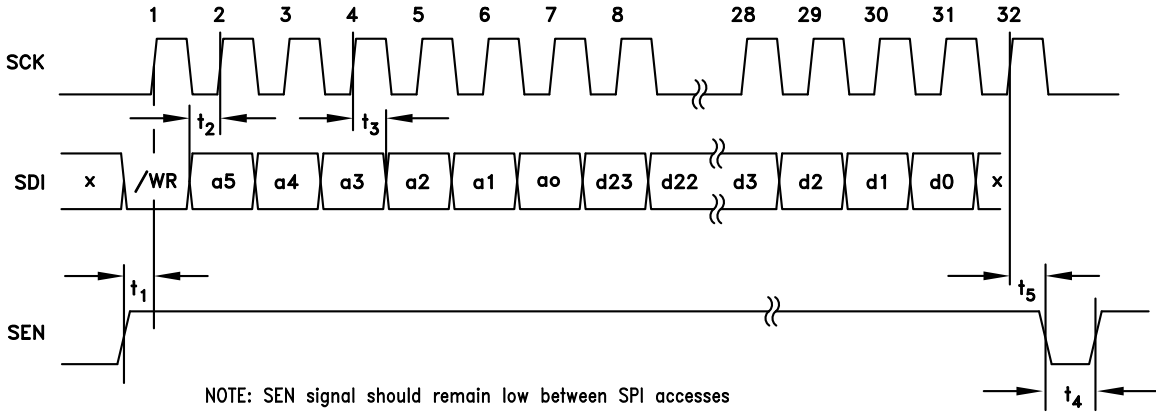


Figure 49. HMC Mode - Serial Port Timing Diagram - WRITE

1.17.3.2 HMC Mode - Serial Port READ Operation

A typical HMC Mode READ cycle is shown in Figure 46.

a. The Master (host) asserts both SEN (Serial Port Enable) and SDI to indicate a READ cycle, followed by a rising edge SCLK. Note: The Lock Detect (LD) function is usually multiplexed onto the LD_SDO pin. It is suggested that LD only be considered valid when SEN is low. In fact LD will not toggle until the first active data bit toggles on LD_SDO, and will be restored immediately after the trailing edge of the LSB of serial data out as shown in Figure 46.

b. The slave (HMC833LP6GE) reads SDI on the 1st rising edge of SCLK after SEN. SDI high initiates the READ cycle (RD)

c. Host places the six address bits on the next six falling edges of SCLK, MSB first.

d. Slave registers the address bits on the next six rising edges of SCLK (2-7).

e. Slave switches from Lock Detect and places the requested 24 data bits on SD_LDO on the next 24 rising edges of SCK (8-31), MSB first .

f. Host registers the data bits on the next 24 falling edges of SCK (8-31).

g. Slave restores Lock Detect on the 32nd rising edge of SCK.

h. De-assertion of SEN completes the cycle

Table 6. SPI HMC Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SEN to SCLK setup time	8			ns
t_2	SDI to SCLK setup time	3			ns
t_3	SCLK to SDI hold time	3			ns
t_4	SEN low duration	20			ns
t_5	SCLK to SDO delay			8.2ns+0.2 ns/pF	ns
t_6	Recovery Time	10			ns

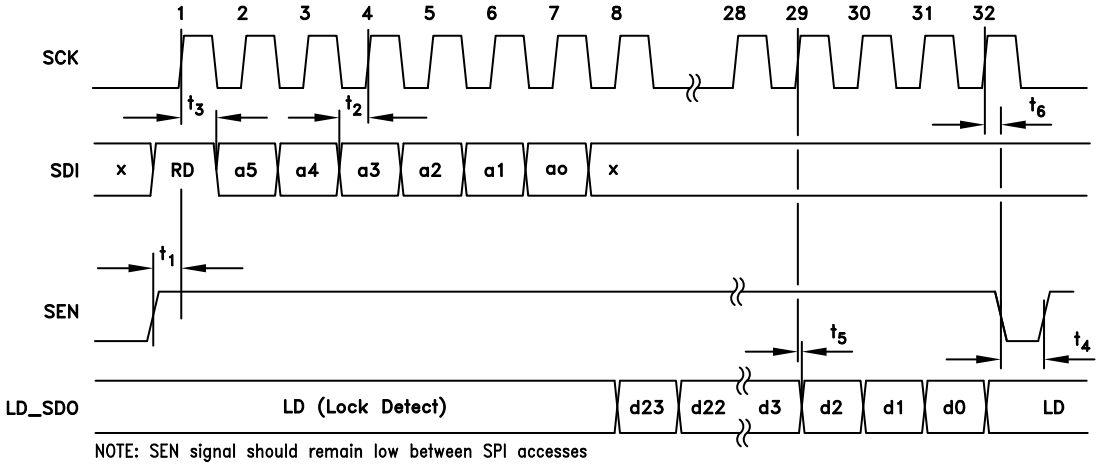


Figure 50. HMC Mode - Serial Port Timing Diagram - READ

1.17.4 Serial Port Open Mode

The Serial Port Open Mode, shown in Figure 47 and Figure 48, features:

a. Compatibility with general serial port protocols that use shift and strobe approach to communication

b. Compatible with Hittite PLL with Integrated VCO solutions, useful to address multiple chips of various types from a single serial port bus.

The Open Mode protocol has the following general features:

a. 3-bit chip address , can address up to 8 devices connected to the serial bus

b. Wide compatibility with multiple protocols from multiple vendors

c. Simultaneous Write/Read during the SPI cycle

d. 5-bit address space

e. 3 wire for Write Only capability, 4 wire for Read/Write capability

Hittite PLLs with integrated VCOs support Open Mode. Some legacy PLL and microwave PLLs with integrated VCOs only support HMC Mode. Consult the relevant data sheets for details.

Typical serial port operation can be run with SCLK at speeds up to 50 MHz.

1.17.4.1 Open Mode - Serial Port WRITE Operation

AVDD = DVDD = 3V ±10%, AGND = DGND = 0V

Table 7. SPI Open Mode - WRITE Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK 32 Rising Edge to SEN Rising Edge	10			ns
t_6	Recovery Time	20			ns
	Max Serial port Clock Speed		50		MHz

A typical WRITE cycle is shown in Figure 47.

a. The Master (host) places 24-bit data, d23:d0, MSB first, on SDI on the first 24 falling edges of SCLK.
b. the slave (HMC833LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK
c. Master places 5-bit register address to be written to, r4:r0, MSB first, on the next 5 falling edges of SCLK (25-29)
d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).
e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32). Hittite reserves chip address a2:a0 = 000 for all RF PLL with Integrated VCOs.
f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).
g. Master asserts SEN after the 32nd rising edge of SCLK.
h. Slave registers the SDI data on the rising edge of SEN.

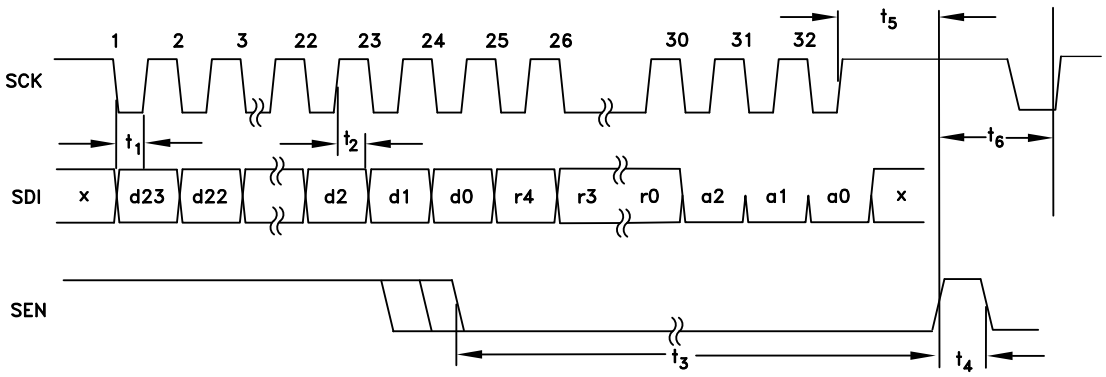


Figure 51. Open Mode - Serial Port Timing Diagram - WRITE

1.17.4.2 Open Mode - Serial Port READ Operation

A typical READ cycle is shown in Figure 48.

In general, in Open Mode the LD_SDO line is always active during the WRITE cycle. During any Open Mode SPI cycle LD_SDO will contain the data from the current address written in Reg0h[7:3]. If Reg0h[7:3] is not changed then the same data will always be present on LD_SDO when an Open Mode cycle is in progress. If it is desired to READ from a specific address, it is necessary in the first SPI cycle to write the desired address to Reg0h[7:3], then in the next SPI cycle the desired data will be available on LD_SDO.

An example of the Open Mode two cycle procedure to read from any random address is as follows:

a. The Master (host), on the first 24 falling edges of SCLK places 24-bit data, d23:d0, MSB first, on SDI as shown in Figure 48. d23:d5 should be set to zero. d4:d0 = address of the register to be READ on the next cycle.
b. the slave (HMC833LP6GE) shifts in data on SDI on the first 24 rising edges of SCLK
c. Master places 5-bit register address , r4:r0, (the READ ADDRESS register), MSB first, on the next 5 falling edges of SCLK (25-29). r4:r0=00000.
d. Slave shifts the register bits on the next 5 rising edges of SCLK (25-29).
e. Master places 3-bit chip address, a2:a0, MSB first, on the next 3 falling edges of SCLK (30-32)..Chip address is always 000 for RF PLL with Integrated VCOs.
f. Slave shifts the chip address bits on the next 3 rising edges of SCLK (30-32).

g. Master asserts SEN after the 32nd rising edge of SCLK.

h. Slave registers the SDI data on the rising edge of SEN.

i. Master clears SEN to complete the the address transfer of the two part READ cycle.

j. If one does not wish to write data to the chip at the same time as we do the second cycle , then it is recommended to simply rewrite the same contents on SDI to Register zero on the READ back part of the cycle.

k. Master places the same SDI data as the previous cycle on the next 32 falling edges of SCLK.

l. Slave (HMC833LP6GE) shifts the SDI data on the next 32 rising edges of SCLK.

m. Slave places the desired read data (ie. data from the address specified in Reg 00h[7:3] of the first cycle) on LD_SDO which automatically switches to SDO mode from LD mode, disabling the LD output.

m. Master asserts SEN after the 32nd rising edge of SCK to complete the cycle and revert back to Lock Detect on LD_SDO.

Table 8. SPI Open Mode - Read Timing Characteristics

Parameter	Conditions	Min.	Typ.	Max	Units
t_1	SDI setup time to SCLK Rising Edge	3			ns
t_2	SCLK Rising Edge to SDI hold time	3			ns
t_3	SEN low duration	10			ns
t_4	SEN high duration	10			ns
t_5	SCLK Rising Edge to SDO time		8.2ns+0.2ns/pF		ns
t_6	Recovery TIme	10			ns
t_7	SCK 32 Rising Edge to SEN Rising Edge	10			ns

1.17.4.3 HMCSPI Open Mode READ Operation - 2 Cycles

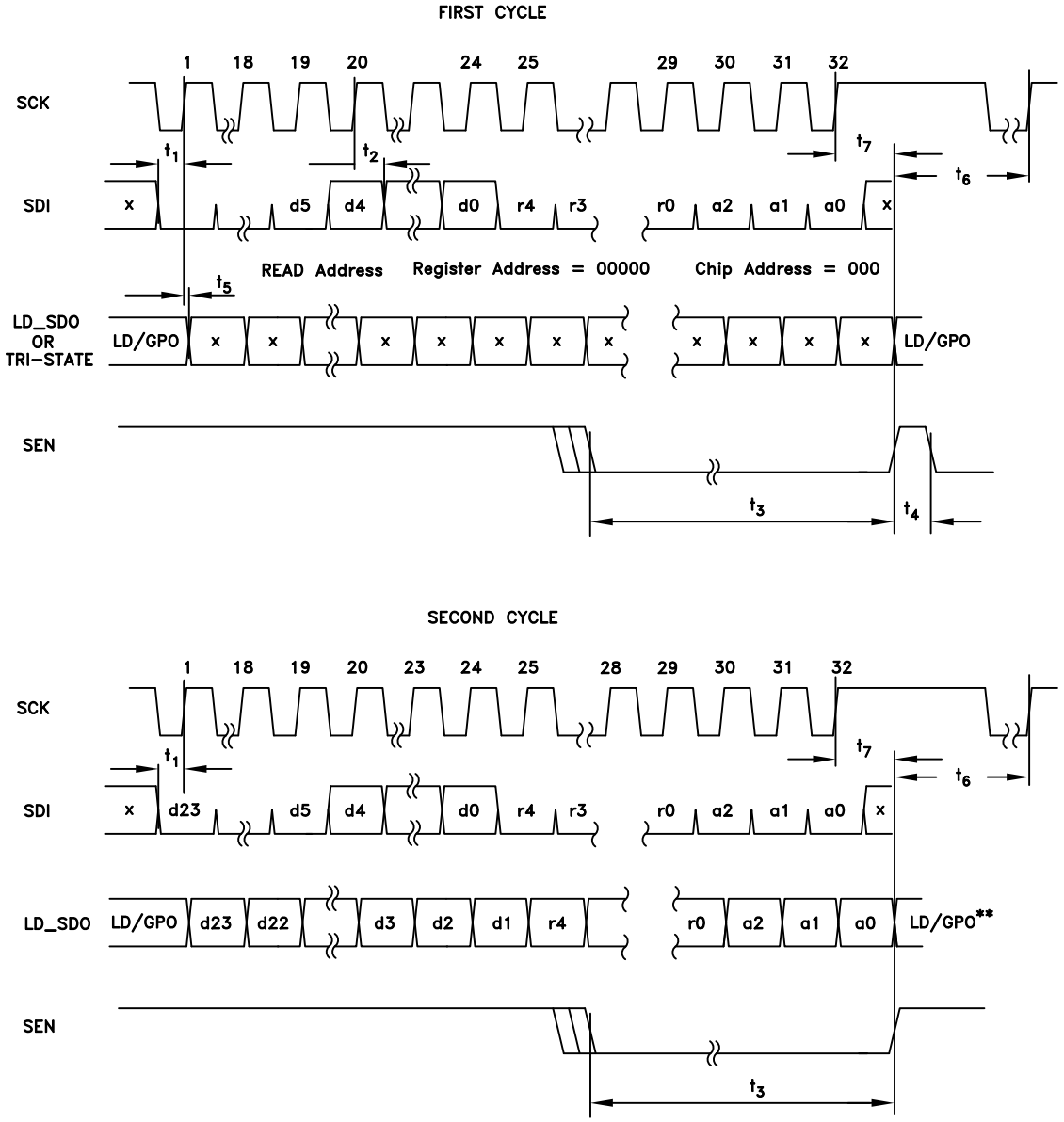


Figure 52. Serial Port Timing Diagram - READ

For more information on using the GPO pin while in SPI Open Mode please see section 1.16.

1.18 Configuration at Start-Up

To configure the PLL after power up, follow the instructions below:

1. Configure the reference divider (write to Reg 02h), if required.

2. Configure the delta-sigma modulator (write to Reg 06h).
   - Configuration involves selecting the mode of the delta-sigma modulator (Mode A or Mode B), selection of the delta-sigma modulator seed value, and configuration of the delta-sigma modulator clock scheme. It is recommended to use the values found in the Hittite PLL evaluation board control software register files.
3. Configure the charge pump current and charge pump offset current (write to Reg 09h)
4. Configure the VCO Subsystem (write to Reg 05h, for more information see section 1.19, and "3.0 VCO Subsystem Register Map". Detailed writes to the VCO subsystem via PLL Reg 05h at start-up are available in the Register Setting Files found in the HIttite PLL Evaluation Software received with a product evaluation kit or downloaded from www.hittite.com.
5. Program the frequency of operation
   - Program the integer part (write to Reg 03h)
   - Program the fractional part (write to Reg 04h)
6. Configure the VCO output divider/doubler, if needed in the VCO subsystem via PLL Reg 05h.

Once the HMC833LP6GE is configured after startup, in most cases the user only needs to change frequencies by writing to Reg 03h integer register, Reg 04h fractional register, and Reg 05h to change the VCO output divider or doubler setting if needed, and possibly adjust the charge pump settings by writing to Reg 09h.

For detailed and most up-to-date start-up configuration please refer to the appropriate Register Setting Files found in the HIttite PLL Evaluation Software received with a product evaluation kit or downloaded from www.hittite.com.

1.19 VCO Serial Port Interface (SPI)

The HMC833LP6GE communicates with the internal VCO subsystem via an internal 16 bit VCO Serial Port, (e.g. see Figure 29). The internal serial port is used to control the step tuned VCO and other VCO subsystem functions, such as RF output divider / doubler control and RF buffer enable.

Note that the internal VCO subsystem SPI (VSPI) runs at the rate of the AutoCal FSM clock, T_{FSM}, (section 1.2.1) where the FSM clock frequency cannot be greater than 50 MHz. The VSPI clock rate is set by Reg 0Ah*[14:13].*

Writes to the VCO's control registers are handled indirectly, via writes to Reg 05h of the PLL. A write to PLL Reg 05h causes the PLL subsystem to forward the packet, MSB first, across its internal serial link to the VCO subsystem, where it is interpreted.

The VCO serial port has the capability to communicate with multiple subsystems inside the IC. For this reason each subsystem has a subsystem ID, Reg 05h[2:0].

Each subsystem has multiple registers to control the functions internal to the subsystem, which may be different from one subsystem to the next. Hence each subsystem has internal register addresses bits (Reg 05h[6:3])

Finally the data required to configure each register within the VCO subsystem is contained in Reg 05h[15:7].

1.19.1 VSPI Use of Reg05h

The packet data written into, Reg 05h is sub-parsed by logic at the VCO subsystem into the following 3 fields:

1. [2:0] - 3 bits - VCO_ID, target subsystem address = 000b.
2. [6:3] - 4 bits - VCO_REGADDR, the internal register address inside the VCO subsystem.
3. [15:7] - 9- bits- VCO_DATA, data field to write into the VCO register.

For example, to write 0_1111_1110 into register 2 of the VCO subsystem (VCO_ID = '000'b), and set the

VCO output divider to divide by 62, the following needs to be written to Reg 05h ='0_1111_1110, 0010, 000' b.

During AutoCal, the AutoCal controller only updates the data field of Reg 05h. The VCO subsystem register address (Reg 05h[6:3]) must be set to 0000 for the AutoCal data to be sent to the correct address.

VCO subsystem ID and register address are not modified by the AutoCal state machine. Hence, if a manual access is done to a VCO Subsystem register the user must reset the register address to zero before a change of frequency which will re-run AutoCal.

Since every write to Reg 05h will result in a transfer of data to the VCO subsystem, if the VCO subsystem needs to be reset manually, it is important to make sure that the VCO switch settings are not changed. Hence the switch settings in Reg 10h[7:0] need to be read first, and then rewritten to Reg 05h[15:8].

In summary, first read Reg 10h, then write to Reg 05h as follows:

Reg 10h[7:0]	= vv x yyyyy
Reg 05h	= vv x yyyyy 0 0000 iii
Reg 05h[2:0]	= iii, subsystem ID, 3 bits (000)
Reg 05h[6:3]	= 0000, subsystem register address
Reg 05h[7]	= 0 , calibration tune voltage off
Reg 05h[12:8]	= yyyyy, VCO caps
Reg 05h[13]	= x, don't care
Reg 05h[15:14]	= vv, VCO Select

2.0 PLL Register Map

2.1 Reg 00h ID Register (Read Only)

Bit	Type	Name	Width	Default	Description
[23:0]	RO	chip_ID	24	A7975	HMC833LP6GE chip ID

2.2 Reg 00h Open Mode Read Address/RST Strobe Register (Write Only)

Bit	Type	Name	Width	Default	Description
[4:0]	WO	Read Address	5	-	(WRITE ONLY) Read Address for next cycle - Open Mode Only
[5]	WO	Soft Reset	1	-	Soft Reset - both SPI modes reset (set to 0 for proper operation)
[23:6]	WO	Not Defined	18	-	Not Defined (set to 0 for proper operation)

2.3 Reg 01h RST Register

(Default 000002h)

Bit	Type	Name	Width	Default	Description
[0]	R/W	rst_chipen_pin_select	1	0	1 = take PLL enable via CEN pin, see Power Down Mode description 0 = take PLL enable via SPI (rst_chipen_from_spi) Reg01[1]
[1]	R/W	rst_chipen_from_spi	1	1	SPI's PLL enable bit
[2]	R/W	Keep_bias_on	1	0	when PLL is disabled, keeps internal bias generators on, ignores chip enable control.
[3]	R/W	Keep_PD_on	1	0	when PLL is disabled, keeps PD circuit on, ignores Chip enable control
[4]	R/W	Keep_CP_on	1	0	when PLL is disabled, keeps Charge Pump on, ignores Chip enable control
[5]	R/W	Keep_Ref_buf_on	1	0	when PLL is disabled, keeps Reference buffer block on, ignores Chip enable control
[6]	R/W	Keep_VCO_on	1	0	when PLL is disabled, keeps VCO divider buffer on, ignores Chip enable control
[7]	R/W	Keep_GPO_driver_on	1	0	when PLL is disabled, keeps GPO output Driver On, ignores Chip enable control
[8]	R/W	Reserved	1	0	Reserved
[9]	R/W	Reserved	1	0	Reserved

2.4 Reg 02h REFDIV Register

(Default 000001h)

Bit	Type	Name	Width	Default	Description
[13:0]	R/W	rdiv	14	1	Reference Divider 'R' Value "(EQ 13)" Divider use also requires refBufEn Reg08[3]=1and Divider min 1d max 16383d

2.5 Reg 03h Frequency Register - Integer Part

(Default 000019h)

Bit	Type	Name	Width	Default	Description
[18:0]	R/W	intg	19	25d	VCO Divider Integer part, used in all modes, see (EQ 13) Fractional Mode min 20d max 2^{19} -4 = 7FFFCh = 524,284d Integer Mode min 16d max 2^{19}-1 = 7FFFFh = 524,287d

2.6 Reg 04h Frequency Register - Fractional Part

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[23:0]	R/W	frac	24	0	VCO Divider Fractional part (24-bit unsigned) see Fractional Frequency Tuning Used in Fractional Mode only (N_{frac}= Reg 04h/2^{24} min 0d max 2^{24}-1

2.7 Reg 05h VCO SPI Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	VCO Subsystem_ID,	3	0	Internal VCO Subsystem ID
[6:3]	R/W	VCO Subsystem register address	4	0	For interfacing with the VCO please see section 1.19.
[15:7]	R/W	VCO Subsystem data	9	0	

Note: Reg05h is a special register used for indirect addressing of the VCO subsystem. Writes to Reg05h are automatically forwarded to the VCO subsystem by the VCO SPI state machine controller.

Reg05h is a Read-Write register. However, Reg05h only holds the contents of the last transfer to the VCO subsystem. Hence it is not possible to read the full contents of the VCO subsystem. Only the content of the last transfer to the VCO subsystem can be read. Please take note special considerations for AutoCal related to Reg05h

2.8 Reg 06h SD CFG Register

(Default 200B4Ah)

Bit	Type	Name	Width	Default	Description
[1:0]	R/W	seed	2	2	Selects the Seed in Fractional Mode 00: 0 seed 01: lsb seed 02: B29D08h seed 03: 50F1CDh seed Note; Writes to this register are stored in the HMC833LP6GE and are only loaded into the modulator when a frequency change is executed and if AutoSeed *Reg06h[8] =1*
[3:2]	R/W	order	2	2	Select the Modulator Type 0: 1st order 1: 2nd order 2: Type 1 Mode B 3: Type 2 Mode A
[6:4]	R/W	Reserved	3	4	Program to 7d
[7]	R/W	frac_bypass	1	0	0: Use Modulator, Required for Fractional Mode, 1: Bypass Modulator, Required for Integer Mode Note: In bypass fractional modulator output is ignored, but fractional modulator continues to be clocked if *frac_rstb =1,* Can be used to test the isolation of the digital fractional modulator from the VCO output in integer mode
[8]	R/W	AutoSeed	1	1	1: loads the seed whenever the frac register is written 0: when frac register write changes frequency, modulator starts with previous contents
[9]	R/W	clkrq_refdiv_sel	1	1	selects the modulator clock source- for Test Only 1: VCO divider clock (Recommended for normal operation) 0: Ref divider clock Ignored if bits [10] or [21] are set
[10]	R/W	SD Modulator Clk Select	1	0	0 - SD auxclk, 1- SD VCO Clock delay (Recommended)
[11]	R/W	SD Enable	1	1	0: disable frac core, use for Integer Mode or Integer Mode with CSP 1: Enable Frac Core, required for Fractional Mode, or Integer isolation testing This register controls whether AutoCal starts on an Integer or a Fractional write
[12]	R/W	Reserved	1	0	
[13]	R/W	Reserved	1	0	
[15:14]	R/W	Reserved	2	0	
[17:16]	R/W	Reserved	2	0	Program to 3d
[18]	R/W	BIST Enable	1	0	Enable Built in Self Test
[20:19]	R/W	RDiv BIST Cycles	2	0	RDiv BIST Cycles 00: 1032 01: 2047 10: 3071 11: 4095
[21]	R/W	auto_clock_config	1	1	Set to 0 for f_{pd} > 50 MHz
[22]	R/W	Reserved	1	0	

2.9 Reg 07h Lock Detect Register

(Default 00014Dh)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	lkd_wincnt_max	3	5d	lock detect window sets the number of consecutive counts of divided VCO that must land inside the Lock Detect Window to declare LOCK 0: 5 1: 32 2: 96 3: 256 4: 512 5: 2048 6: 8192 7: 65535
[3]	R/W	Enable Internal Lock Detect	1	1	see section 1.16
[5:4]	R/W	Reserved	2	0	Reserved
[6]	R/W	Lock Detect Window type	1	1	Lock Detection Window Timer Selection 1: Digital programmable timer 0: Analog one shot, nominal 10 ns window
[9:7]	R/W	LD Digital Window duration	3	2	0 Lock Detection - Digital Window Duration 0: 1/2 cycle 1: 1 cycle 2: 2 cycles 3: 4 cycles 4: 8 cycles 5: 16 cycles 6: 32 cycles 7: 64 cycles
[11:10]	R/W	LD Digital Timer Freq Control	2	0	Lock Detect Digital Timer Frequency Control “00” fastest “11” slowest
[12]	R/W	LD Timer Test Mode	1	0	1: force Timer Clock ON Continuously - For Test Only 0: Normal Timer operation - one shot
[13]	R/W	Auto Relock - One Try	1	0	1: Attempts to relock if Lock Detect fails for any reason Only tries once.

2.10 Reg 08h Analog EN Register

(Default C1BEFFh)

Bit	Type	Name	Width	Default	Description
[0]	R/W	bias_en	1	1	Enables main chip bias reference
[1]	R/W	cp_en	1	1	charge pump enable
[2]	R/W	PD_en	1	1	PD enable
[3]	R/W	refbuf_en		1	Reference path buffer enable
[4]	R/W	vcobuf_en	1	1	VCO path RF buffer enable
[5]	R/W	gpo_pad_en	1	1	0 - Pin LD_SDO disabled 1 - and RegFh[7]=1 , Pin LD_SDO is always on required for use of GPO port 1 - and RegFh[7]=0 SPI LDO_SPI is off if unmatched chip address is seen on the SPI, allowing a shared SPI with other compatible parts
[6]	R/W	reserved	1	1	reserved
[7]	R/W	VCO_Div_Clk_to_dig_en	1	1	VCO Divider Clock to Digital Enable
[8]	R/W	reserved	1	0	reserved
[9]	R/W	Prescaler Clock enable	1	1	Prescaler clock enable
[10]	R/W	VCO Buffer and Prescaler Bias Enable	1	1	VCO Buffer and Prescaler Bias Enable
[11]	R/W	Charge Pump Internal Opamp enable	1	1	Should be programmed to 1
[14:12]	R/W	reserved	3	011	reserved
[17:15]	R/W	reserved	3	011	reserved
[18]	R/W	spare	1	0	spare
[19]	R/W	reserved	1	0	reserved
[20]	R/W	reserved	1	0	reserved program to 0
[21]	R/W	High Frequency Reference	1	0	Program to 1 for XTAL > 200 MHz
[22]	R/W	reserved	1	1	reserved program to 1
[23]	R/W	reserved	1	1	reserved program to 1

2.11 Reg 09h Charge Pump Register

(Default 403264h)

Bit	Type	Name	Width	Default	Description
[6:0]	R/W	CP DN Gain	7	100d 64h	Charge Pump DN Gain Control 20 µA/step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA
[13:7]	R/W	CP UP Gain	7	100d 64h	Charge Pump UP Gain Control 20 µA per step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 20 µA 2d = 40 µA ... 127d = 2.54mA
[20:14]	R/W	Offset Magnitude	7	0	Charge Pump Offset Control 5 µA/step Affects fractional phase noise and lock detect settings 0d = 0 µA 1d = 5 µA 2d = 10 µA ... 127d = 635 µA
[21]	R/W	Offset UP enable	1	0	recommended setting = 0
[22]	R/W	Offset DN enable	1	1	recommended setting = 1 in Fractional Mode, 0 otherwise
[23]	R/W	HiKcp	1	0	HiKcp High Current Charge Pump

2.12 Reg 0Ah VCO AutoCal Configuration Register

(Default 002205h)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	Vtune Resolution	3	5	R Divider Cycles 0 - 1 1 - 2 2 - 4 ... 7 - 256
[5:3]	R/W	VCO Curve Adjustment	3	0	VCO Curve Adjustment vs Temp for AutoCal 0 - Disabled 1 : + 1 Curve 2: +2 Curves 3: +3 Curves 4: -4 Curves 5: -3 Curves 6: -2 Curves 7: -1 Curve
[7:6]	R/W	Wait State Set Up	2	0	Wait State Setup 100 T_{FSM} see section 1.2.4 T_{mmt} = 1 measurement cycle of AutoCal 0: Wait Only at Startup 1: Wait on startup and after first T_{mmt} cycle 2: Wait on startup and after first two T_{mmt} cycles 3: Wait on startup and after first three T_{mmt} cycles
[9:8]	R/W	Num of SAR BIts in VCO	2	0	Number of SAR bits in VCO 0: 8 - recommended 1: 7 2: 6 3: 5
[10]	R/W	Force Curve	1	0	Force curve sent during Tuning Tune from Reg5
[11]	R/W	Bypass VCO Tuning	1	0	Bypass VCO Tuning
[12]	R/W	No VSPI Trigger	1	0	Don't trigger a transfer on writes to Reg 05h
[14:13]	R/W	FSM/VSPI Clock Select	2	1	Set the AutoCal FSM and VSPI Clock (50 MHz maximum) 0: Input Crystal Reference 1: Input Crystal Reference/4 2: Input Crystal Reference/16 3: Input Crystal Reference/32
[15]	R/W	Xtal Falling Edge for FSM	1	0	Use the falling Edge of the Xtal for FSM AutoCal Clock - Required for BIST
[16]	R/W	Force RDivider Bypass	1	0	Force the R Divider Bypass

2.13 Reg 0Bh PD Register

(Default 7C061h)

Bit	Type	Name	Width	Default	Description
[2:0]	R/W	PD_del_sel	3	1	Sets PD reset path delay (Recommended setting 001)
[3]	R/W	Short PD Inputs	1	0	Shorts the inputs ot the Phase frequency detector - Test Only
[4]	R/W	pd_phase_sel	1	0	Inverts the PD polarity (program to 0) 0- Use with a positive tuning slope VCO and Passive Loop Filter (default) 1- Use with a Negative Slope VCO or with an inverting Active Loop Filter with a Positive Slope VCO
[5]	R/W	PD_up_en	1	1	Enables the PD UP output
[6]	R/W	PD_dn_en	1	1	Enables the PD DN output
[8:7]	R/W	CSP Mode	2	0	Cycle Slip Prevention Mode Extra current is driven into the loop filter when the phase error is larger than: 0: Disabled 1: 5.4ns 2: 14.4ns 3: 24.1ns This delay varies by +- 10% with temperature, and +- 12% with process.
[9]	R/W	Force CP UP	1	0	Forces CP UP output on - Use for Test only
[10]	R/W	Force CP DN	1	0	Forces CP DN output on - Use for Test only
[11]	R/W	Force CP MId Rail	1	0	Force CP MId Rail - Use for Test only
[14:12]	R/W	Reserved	3	4	program to 100
[16:15]	R/W	CP Internal OpAmp Bias	2	3	program to 11
[18:17]	R/W	MCounter Clock Gating	2	3	MCounter Clock Gating 0: MCounter Off 1: N<128 2: N< 1023 3: All Clocks ON (Recommended setting 11)
[19]	R/W	reserved	1	0	program to 0
[21:20]	R/W	reserved	2	0	program to 00
[23:22]	R/W	reserved	2	0	program to 00

2.14 Reg 0Ch Exact Frequency Mode Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[13:0]	R/W	Number of Channels per Fpd	14	0	Comparison Frequency divided by the Correction Rate, Must be an integer. Frequencies at exactly the correction rate will have zero frequency error. 0: Disabled 1: Disabled 2:16383d (3FFFh)

2.15 Reg 0Fh GPO_SPI_RDIV Register

(Default 000001h)

Bit	Type	Name	Width	Default	Description
[4:0]	R/W	gpo_select	5	1d	Signal selected here is output to SDO pin when enabled 0: Data from Reg0F[5] 1: Lock Detect Output 2. Lock Detect Trigger 3: Lock Detect Window Output 4: Ring Osc Test 5. Pullup Hard from CSP 6. PullDN hard from CSP 7. Reserved 8: Reference Buffer Output 9: Ref Divider Output 10: VCO divider Output 11. Modulator Clock from VCO divider 12. Auxiliary Clock 13. Aux SPI Clock 14. Aux SPI Enable 15. Aux SPI Data Out 16. PD DN 17. PD UP 18. SD3 Clock Delay 19. SD3 Core Clock 20. AutoStrobe Integer Write 21. Autostrobe Frac Write 22. Autostrobe Aux SPI 23. SPI Latch Enable 24. VCO Divider Sync Reset 25. Seed Load Strobe 26.-29 Not Used 30. SPI Output Buffer En 31. Soft RSTB
[5]	R/W	GPO Test Data	1	0	1 - GPO Test Data
[6]	R/W	Prevent Automux SDO	1	0	1- Outputs GPO data only 0 - Automuxes between SDO and GPO data
[7]	R/W	LDO Driver Always On	1	0	1- LD_SDO Pin Driver always on 0 - LD_SDO Pin driver only on during SPI read cycle
[8]	R/W	Disable PFET	1	0	program to 0
[9]	R/W	Disable NFET	1	0	program to 0

2.16 Reg 10h VCO Tune Register

(Default 000020h)

Bit	Type	Name	Width	Default	Description
[7:0]	RO	VCO Switch Setting	8	32	Read Only Register. Indicates the VCO switch setting selected by the AutoCal state machine to yield the nearest free running VCO frequency to the desired operating frequency. Not valid when Reg10h[8] = 1, AutoCal Busy. Note if a manual change is done to the VCO switch settings this register will not indicate the current VCO switch position. 0 = highest frequency 1 = 2nd highest ... 256 = lowest frequency Note: VCO subsystems may not use all the MSBs, in which case the unused bits are don't care
[8]	RO	AutoCal Busy	1	0	Busy when AutoCal state machine is searching for the nearest switch setting to the requested frequency.

2.17 Reg 11h SAR Register

(Default 007FFFh)

Bit	Type	Name	Width	Default	Description
[18:0]	RO	SAR Error Mag Counts	19	2^{19}-1	SAR Error Magnitude Counts
[19]	RO	SAR Error Sign	1	0	SAR Error Sign 0=+ve 1=-ve

2.18 Reg 12h GPO2 Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[0]	RO	GPO	1	0	GPO State
[1]	RO	Lock Detect	1	0	Lock Detect Status 1 = Locked 0 = Unlocked

2.19 Reg 13h BIST Register

(Default 000000h)

Bit	Type	Name	Width	Default	Description
[15:0]	RO	BIST Signature	19	4697d	BIST Signature
[16]	RO	BIST Busy	1	0	BIST Busy

3.0 VCO Subsystem Register Map

Please note that the VCO subsystem uses indirect addressing via Reg 05h. For more detailed information on how to write to the VCO subsystem please see section "1.19 VCO Serial Port Interface (SPI)".

3.1 VCO_Reg 00h Tuning

Bit	Type	Name	Width	Default	Description
[0]	WO	Cal	1	0	VCO tune voltage is redirected to a temperature compensated calibration voltage
[8:1]	WO	CAPS	8	16	VCO sub-band selection. 0 - max frequency 1111 1111 - min frequency. Not all sub-bands are used on the various products.

3.2 VCO_Reg 01h Enables

Bit	Type	Name	Width	Default	Description
[0]	WO	Master Enable VCO Subsystem	1	1	0 - All VCO subsystem blocks Off Manual mode (VCO_Reg 03h[2] = 1) 1- ANDed with local enables only Auto Mode (VCO_Reg 03h[2] = 0) 1- Master enable ignores local enables
[1]	WO	Manual Mode PLL buffer enable	1	1	Enables PLL Buffer in manual mode only
[2]	WO	Manual Mode RF buffer enable	1	1	Enables RF Buffer to Output in manual mode only
[3]	WO	Manual Mode Divide by 1 enable	1	1	Enables RF divide by 1 in manual mode only
[4]	WO	Manual Mode RF Divider enable	1	1	Enables RF divider in manual mode only
[8:5]	WO	don't care	4	0	don't care

For example, to turn disable the RF buffer in the VCO subsystem and mute the output of the HMC833LP6GE, bit 2 in VCO_Reg01h needs to be cleared. If the other bits are left unchanged, then '0 0001 1011' needs to be written into VCO Reg01h. The VCO subsystem register is accessed via a write to PLL subsystem Reg 05h = '0 0001 1011 0001 000' = D88h

Reg 05h[2:0] = 000; VCO subsystem ID 0
Reg 05h[6:3] = 0001; VCO subsystem register address
Reg 05h[7] = 1; Master enable
Reg 05h[8] = 1; PLL buffer enable
Reg 05h[9] = 0; Disable RF buffer
Reg 05h[10] = 1; Divide by 1 enable
Reg 05h[11] = 1; RF Divider enable
Reg 05h[16:12] = 0; don't care

3.3 VCO_Reg 02h Biases

Bit	Type	Name	Width	Default	Description
[5:0]	WO	RF Divide ratio	6	1	0 - Mute, VCO and PLL buffer On, RF output stages Off 1 - Fo 2 - Fo/2 3 - invalid, defaults to 2 4 - Fo/4 5 - invalid, defaults to 4 6 - Fo/6 ... 60 - Fo/60 61 - invalid, defaults to 60 62 - Fo/62 > 62 - invalid, defaults to 62 Note: This register automatically controls the enables to the, RF output buffer, RF divider, RF divide by 1 path, and requires Master Enable (VCO_Reg 01h[0] = 1) and AutoRFO mode (VCO_Reg 03h [2] = 0) Note: bit[0] is a don't care in ManualRFO mode.
[7:6]	WO	RF output buffer gain control	2	3	11 - Max Gain 10 - Max Gain - 3 dB 01 - Max Gain - 6 dB 00 - Max Gain - 9 dB
[8]	WO	Divider output stage gain control	1	0	1 - Max Gain 0 - Max Gain - 3 dB Used to flatten the output power level across frequency • For divide-by 1 or divide-by 2 it is recommended to set this bit to 1. 0 will reduce output power and degrade noise floor performance. • For divide-by 4 or higher, it is recommended to set this bit to 0 to maintain flat output power across divider settings. Setting this bit to 1, with divide-by 4 or higher provides higher output power compared to the divide-by 1 or two case.

For example, to write 0_1111_1110 into VCO_Reg02h VCO subsystem (VCO_ID = '000'b), and set the VCO output divider to divide by 62, the following needs to be written to Reg 05h ='0_1111_1110, 0010, 000' b.

Reg 05h[2:0] = 00; subsystem ID 0
Reg 05h[6:3] = 0010; VCO register address 2d
Reg 05h[16:7] = 0_1111_1110; Divide by 62, max output RF gain, Divider output stage gain = 0

3.4 VCO_Reg 03h Config

Bit	Type	Name	Width	Default	Description
[0]	WO	Fundamental/Doubler Mode Selection	1	1	0- Enable the frequency doubler mode of operation 1- Enable fundamental mode of operation - For more information please see "VCO Subsystem" section.
[1]	WO	reserved	1	0	reserved
[2]	WO	Manual RFO Mode	1	0	0 - AutoRFO mode (recommended) 1 - ManualRFO mode AutoRFO mode controls output buffers and RF divider enables according to RF divider setting in VCO_Reg 02h[5:0] ManualRFO mode requires manual enables of individual blocks via VCO_Reg01h
[4:3]	WO	RF buffer bias	2	0	Program to '10'b for output frequencies < 3000 MHz (when VCO_Reg03h[0] = 1)

3.4 VCO_Reg 03h Config

Bit	Type	Name	Width	Default	Description
[8:5]	WO	Spare	4	2	Program to '00'b for output frequencies > 3000 MHz, (when VCO_Reg03h[0] = 0)

3.5 VCO_Reg 04h Cal/Bias

Specified performance is only guaranteed with the required settings in this table. Other settings are not supported.

Bit	Type	Name	Width	Default	Description
[2:0]	WO	VCO bias	3	1	Program to 1d
[4:3]	WO	PLL buffer bias	2	1	Program to 0d
[6:5]	WO	FndLmtr bias	2	2	Program to 2d
[8:7]	WO	Preset Cal 0	2	1	Program to 1d

3.6 VCO_Reg05h CF_Cal

Bit	Type	Name	Width	Default	Description
[1:0]	WO	CF L	2	2	Program to 0d
[3:2]	WO	CF ML	2	2	Program to 3d
[5:4]	WO	CF MH	2	2	Program to 2d
[7:6]	WO	CF H	2	2	Program to 0d
[8]	WO	Spare	1	0	Program to 0d

3.7 VCO_Reg06h MSB Cal

Bit	Type	Name	Width	Default	Description
[1:0]	WO	MSB L	2	3	Program to 3d
[3:2]	WO	MSB ML	2	3	Program to 3d
[5:4]	WO	MSB MH	2	3	Program to 3d
[7:6]	WO	MSB H	2	3	Program to 3d
[8]	WO	Spare	1	0	don't care

NOTES: